3A Ultra Low Dropout Regulator with Enable

General Description

The AP1313 are high performance positive voltage regulators designed for using in applications requiring very low input voltage and very low dropout voltage up to 3 A output current. It can operate down to VIN = 1.2 V and VCNTL = 3.2 V with output voltage programmable as low as 0.8 V. The AP1313 feature ultra-low dropout, ideal for applications where output voltage is very close to input voltage.

Additionally, the AP1313 integrated an enable input to further reduce power dissipation while shutdown. Also, it provided an excellent regulation over variations in line, load and temperature. The AP1313 has a power ready signal 'POK' to indicate the output status if the voltage level of output reaches 92 % of its nominal value. The AP1313 are available in the thermally enhanced SO8-EP and DFN3x3-10 packages.

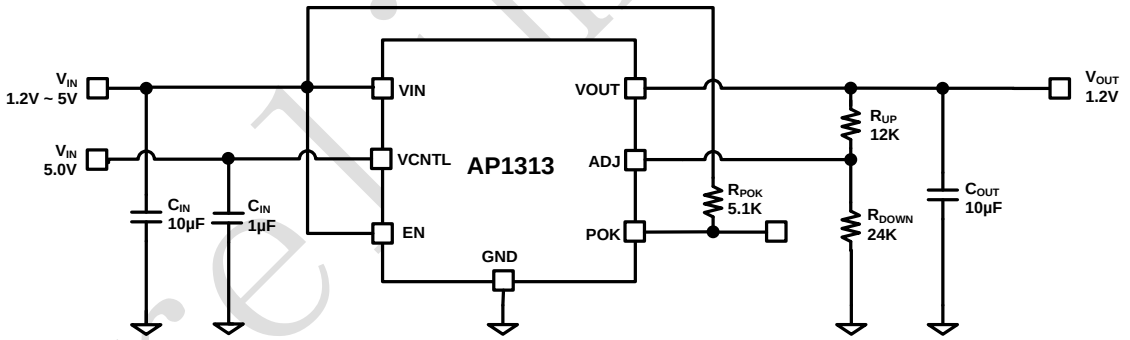
Features

- Ultra-low Dropout
- 3A Current with 230 mV Dropout only at VOUT = 1.2 V
- Adjust Output Voltage Externally down to 0.8 V by Setting VADJ above 0.2 V
- Low ESR Output Capacitor Applicable
- Input Voltage as Low as 1.2 V
- VCNTL Voltage Down to 3.2 V
- Output Voltage Accuracy to ±1.5 % (Internal Default Voltage)
- Low VCNTL Shutdown Quiescent Current ~ 5 μA
- Enable Input for Power Sequencing
- Internal Soft-start
- Open Drain Power OK Indicator
- VOUT Pull Low Resistance when Disable
- Over Current and Over Temperature Protections
- SO8-EP and DFN3x3-10 Packages
- Lead Free and Green Device Available

Applications

- Motherboard Computers
- Peripheral Cards
- Network Cards
- Set Top Boxe

Typical Application Circuit

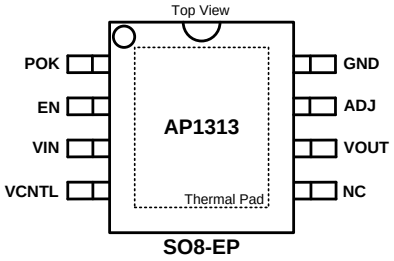


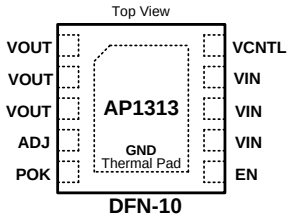
Ordering Information

Order Codes	Default VOUT	Packages	Shipping	Top Markings(1)
AP1313SP-A1	ADJ	SO8-EP	4,000 /Reel	AP1313 YWWXXXXX
AP1313DF-A1		DFN-10	5,000 /Reel	1313 YWWXX

(1). YWW = Date code

Pin Configurations





Pin Description

Pin No.		Pin Names	Pin Functions
SO8-EP	DFN-10		
1	5	POK	Power OK pin is open drain output. Once VOUT hit 92% of its rating voltage. The POK pin will high.
2	6	EN	Driving the enable pin (EN) over 1.0V turns on the regulator. Driving this pin below 0.4V, the regulator into shutdown mode, VIN power reducing operating current to 1μA typical.
3	7,8,9	VIN	Input power pin. A small capacitor is needed from this pin to ground to assure stability. Typical input ~10μF. Both input and output capacitor grounds should be tied back to the IC ground with no significant impedance between them.
4	10	VCNTL	Input pin for control circuit power. Typical use 1μF capacitor connect between this pin to ground.
5	-	NC	Not connected.
6	1,2,3	VOUT	Regulated output voltage pin. A small (10μF) ceramic capacitor is needed from this pin to ground to assure stability. A pull low discharge resistance exists when deactivate device by VEN.
7	4	ADJ	Connect this pin to ground, the output voltage by the internal feedback resistors. If external feedback resistors are used, the output voltage will be V_{OUT} = 0.8(R1+R2)/R2 Volts.
8	DAP (11)	GND	Ground pin.

Table 1

Functional Block Diagram

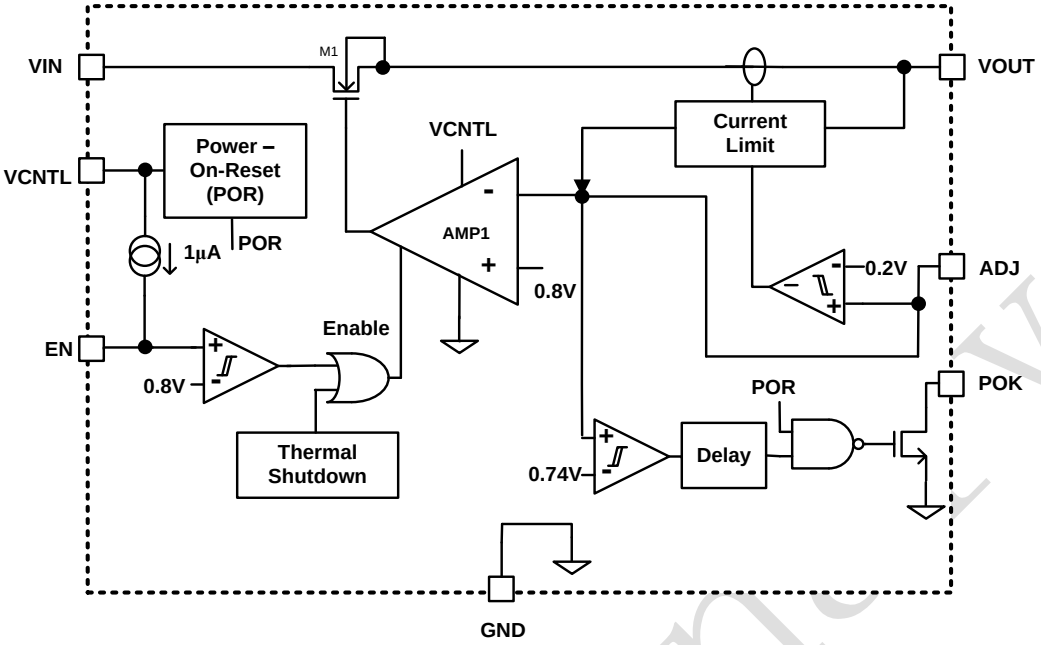


Figure 1. Functional Block Diagram

Absolute Maximum Ratings (1)

VCNTL, POK, EN, VADJ.....-0.3 V ~ 6.0 V
VIN, VOUT.....-0.3 V ~ 5.5 V
ESD protection Rating
Human Body Model (HBM).....±2kV(2)
Machine Model (MM).....200V(3)
Charged Device Model (CDM).....1kV(4)
Package Thermal Resistance(5)
Θ_{JA}, SO8-EP.....60 ℃/W
Θ_{JC}, SO8-EP.....14 ℃/W
Θ_{JA}, DFN-10.....68 ℃/W
Θ_{JC}, DFN-10.....8 ℃/W

Maximum Power Dissipation(6)
SO8-EP.....2.1 W
DFN-10.....1.47 W
Min. Operating T_J.....-40 ℃
Max. Operating T_J.....Internally Limited
Storage Temperature.....-55 ℃ ~ 150 ℃
Lead Temperature (Soldering 10 sec.)……...260 °C

(1). Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.
(2). Tested and classified as Class 2 per ESDA/JEDEC JDS-001-2014.
(3). Tested and classified as M3 per Standard ANSI/ESDA/JEDEC Test Method A115-B-2010.
(4). Tested and classified as Class 4 per ESDA/JEDEC 22-C101E-2009.
(5). Thermal Resistance is measured in the natural convection at TA = 25 ℃ on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard.
(6). The maximum power dissipation (PD) is given by the following formula: $PD=\frac{T_{JMAX}-T_A}{R_{\theta JA}}$

Electrical Characteristics (1)

(V_{CNTL} = V_{EN} = 5 V, V_{IN} =3.3 V, I_{OUT} = 10 mA, C_{IN}=10 µF, C_{OUT} = 10 µF, T_A = 25 ℃, unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Supply Voltage						
VIN Input Voltage Range	V_{IN}	V_{OUT} = 0.8V	1.2		5	V
VIN Quiescent Current	I_{VIN_Q}	V_{OUT} = 2.5V		20	50	µA
VIN Shutdown Current	I_{VIN_SD}	V_{EN} = 0V			1	µA
VIN UVLO Rising Threshold	V_{IN_UVLO}		0.8		1.2	V
VIN UVLO Hysteresis	V_{IN_HYS}			0.45		V
VCNTL Input Control Voltage						
Control Supply Voltage Range	V_{CNTL}		3.2		5.5	V
VCNTL Quiescent Current	I_{VCNT_Q}	VOUT = 2.5V		270	350	µA
VCNTL Shutdown Current	I_{VCNTL_SD}	V_{EN} = 0V		5	10	µA
VCNTL UVLO Rising Threshold	V_{CNT_LUVLO}		2.5	2.7	3.2	V
VCNTL UVLO Hysteresis	V_{CNT_HYS}			0.6		V
Output Voltage and Current Limit						
Output Voltage Range	V_{OUT}	V_{IN} = 3.3V	0.8		2.5	V
Line Regulation	REG_{LINE}	V_{IN} = V_{OUT} + 0.5V to 3.3V		0.1	0.15	%
Load Regulation(2)	REG_{LOAD}	10mA to 3A		0.2		%
Drop Voltage (2)	V_{DROP}	I_{OUT} = 3A -40 to 125 ℃		230	300	mV
Current Limit	I_{LIMIT_NORMAL}	V_{ADJ} > 0.2V	3.6	4.3	5	A
Short Circuit Current Limit	I_{LIMIT_SHORT}	V_{ADJ} < 0.2V, V_{IN}=3.3V		1.4		A
Short Circuit Blanking Time(2)	T_{ILIMIT}			5		ms
VOUT Discharge Resistance(2)	R_{DIS}			90		Ω

Electrical Characteristics (1) (continued)

(V_{CNTL} = V_{EN} = 5 V, V_{IN} =3.3 V, I_{OUT} = 10 mA, C_{IN}=10 µF, C_{OUT} = 10 µF, T_A = 25 ℃, unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output Voltage						
Feedback Reference Voltage	V_{REF}	V_{ADJ} = V_{OUT}	0.788	0.800	0.812	V
Feedback Pin Current	I_{ADJ}		-100		100	nA
Internal Feedback Control Threshold(2)	V_{TH_ADJ}		0.15	0.2	0.25	V
Enable and Soft-start						
EN Pins High Level Input Voltage	V_{EN_HI}		1.1			V
EN Pins Low Level Input Voltage	V_{EN_LO}				0.4	V
EN Pins Pull Up Current	I_{EN}	V_{EN} = 0V		1.7	4	µA
Turn ON Delay(2)				450		µs
Soft-Start Time				1.5		ms
POK and Delay						
Power Good High Threshold	V_{TH_POK}			92		%
Power Good Hysteresis	V_{HYS_POK}			2		%
Power Good Delay Time	T_{POK}		-	1.3	-	ms
Thermal Shutdown						
Thermal Shutdown Threshold(2)	T_{SD}		130			℃
Thermal Shutdown Hysteresis(2)	T_{SD_HYS}			30		℃

(1). Specifications over temperature range are guaranteed by design and characterization.
(2). Guaranteed by design and characterization only.

Functional Description

Power-On-Reset

A Power-On-Reset (POR) circuit monitors both of supply voltages on VCNTL and VIN pins to reset a logic controls. The POR function initiates a soft-start process after both of the supply voltages exceed their rising POR voltage thresholds during powering on. The POR function also pulls low the POK voltage regardless the output status when one of the supply voltages falls below its falling POR voltage threshold.

Internal Soft Start

An internal soft-start function controls rise rate of the output voltage to limit the current surge during start-up. The typical soft-start interval is about 1.5ms.

Output Voltage Regulation

An error amplifier works with a temperature-compensated 0.8V reference and an output NMOS regulates output to the preset voltage. The error amplifier is designed with high bandwidth and DC gain provides very fast transient response and good load regulation. It compares the reference with the feedback voltage and amplifies the difference to drive the output NMOS which provides load current from VIN to VOUT.

The AP1313 monitors the current flowing through the output NMOS and limits the maximum current to prevent load. AP1313 also provided a short current-limit and auto restart function, it will change the current-limit level down to 1.4 A (typ) when the voltage on FB pin falls below 0.2V (typ) during current overload or short circuit conditions. However, start up with enable (EN) pin, the short circuit current-limit will disabled until Soft-start interval finished.

Enable Control

The AP1313 has a dedicated enable pin (EN). A logic low signal applied to this pin shuts down the output. Following a shutdown, a logic high signal re-enables the output through initiation of a new soft-start cycle. When left open, this pin is pulled up by an internal current source (1.7 µA typical) to enable normal operation. It's not necessary to use an external transistor to save cost.

Power-OK and Delay

The AP1313 indicates the status of the output voltage by monitoring the feedback voltage (VFB) on POK pin. As the VFB rises and reaches the rising Power-OK voltage threshold (VTHPOK), an internal delay function starts to work. At the end of the delay time, the IC turns off the internal NMOS. POK pin will indicate high when the output is ok. As the VFB falls and reaches the falling Power-OK voltage threshold, the IC turns on the NMOS of the POK. Also, if the VIN or VCNTL lower than POR threshold. The POK pin will pull low.

Application Information

Power Sequencing

The power sequencing of VIN and VCNTL is not necessary to be concerned. However, do not apply a voltage to VOUT for a long time when the main voltage applied at VIN is not present. Because the output auto discharger switch will turn on when VIN is not present.

Input Capacitor

The AP1313 requires proper input capacitors to supply current surge during stepping load transients to prevent the input voltage rail from dropping. Because the parasitic inductor from the voltage sources or other bulk capacitors to the VIN pin limit the slew rate of the surge currents, more parasitic inductance needs more input capacitance. Ultra-low-ESR capacitors (such as ceramic chip capacitors) and low-ESR bulk capacitors (such as solid tantalum, POSCap, and Aluminum electrolytic capacitors) can all be used as an input capacitor of VIN. For most applications, the recommended input capacitance of VIN is 10μF at least. However, if the drop of the input voltage is not cared, the input capacitance can be less than 10μF.

Output capacitor

The AP1313 is designed specifically to work with low ESR ceramic output capacitor for space saving. A ceramic capacitor with capacitance of at least 4.7μF and ESR larger than 1mΩ are recommend. Large output capacitor can reduce noise and improve load transient response. Figure 2 shows the allowable ESR range as function of load current various output capacitance.

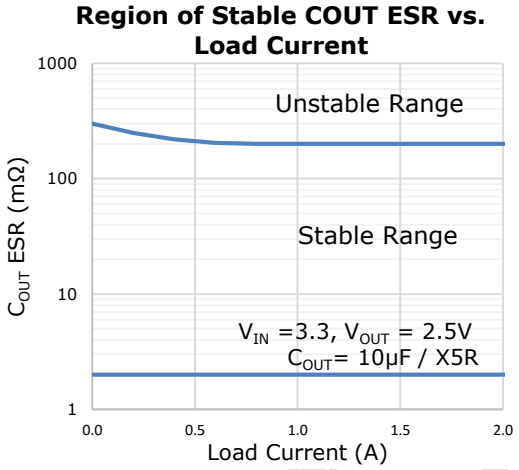


Figure 2

Setting Output Voltage

The output voltage is programmed by the resistor divider connected to FB pin. The preset output voltage is calculated by the following equation:

$$VOUT=0.8V \times \left(1+\frac{Rup}{Rdown}\right) \quad \text{.....(1)}$$

Where R_{UP} is the resistor connected from VOUT to FB pin with Kelvin sensing connection and R_{DOWN} is the resistor connected from FB to GND.

Layout Consideration

1. Solder the exposed pad on the VIN ground pad on the top-layer of PCBs. The VIN or ground pad must have wide size to conduct heat into the ambient air through the VIN or ground plane and PCB as a heat sink.
2. Please place the input capacitors for VIN and VCNTL pins near the pins as close as possible for decoupling high-frequency ripples.
3. Please the feedback resistors R_{UP} and R_{DOWN} near the AP1313 as close to avoid noise coupling.
4. The input and output capacitors and GND pin must be connected to ground plane of the load.
5. Figure 4. Bottom Layer Figure 3. Top Layer Large current paths must have wide tracks.

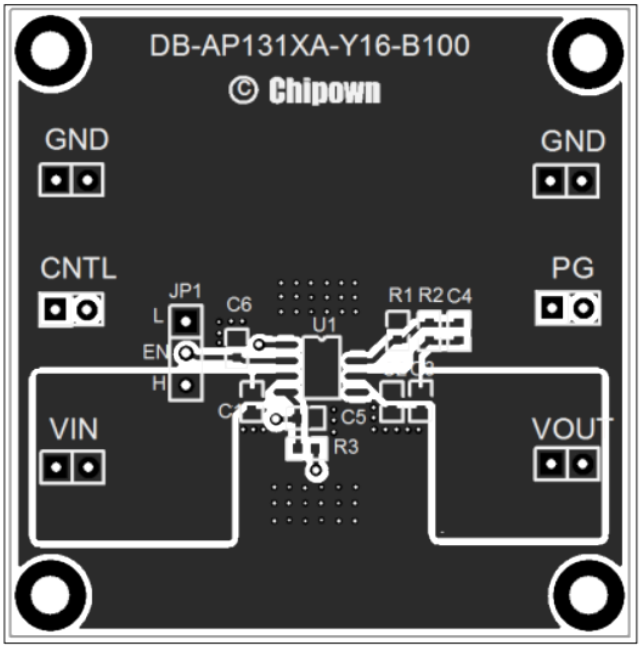


Figure 3. Top Layer

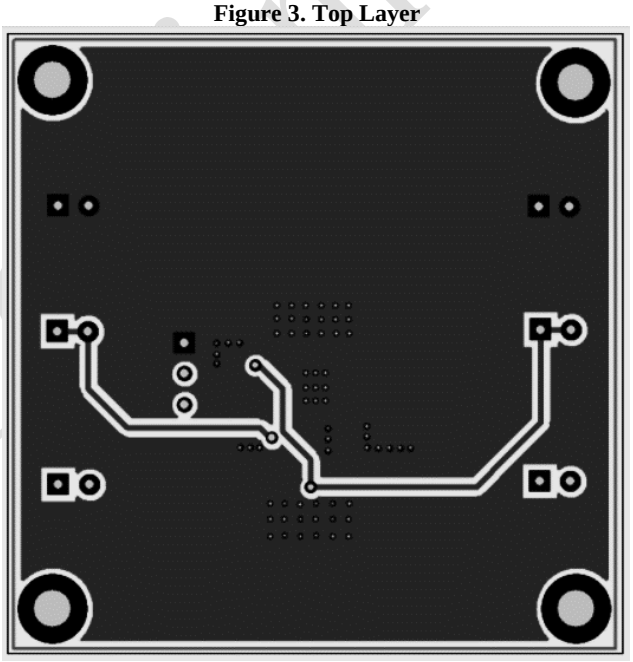


Figure 4. Bottom Layer

Typical Performance Characteristics

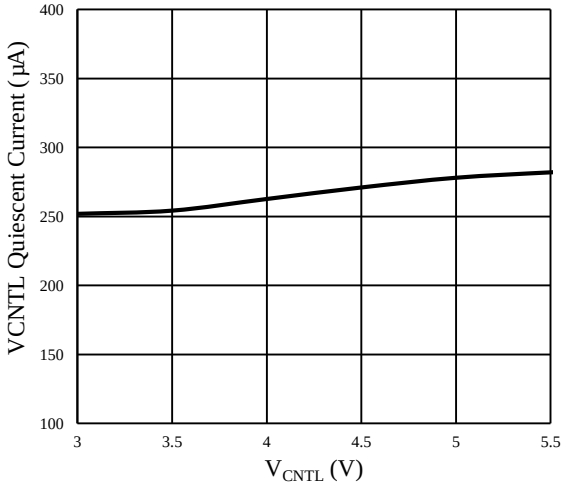


Figure 5. VCNTL Current vs. Input Voltage

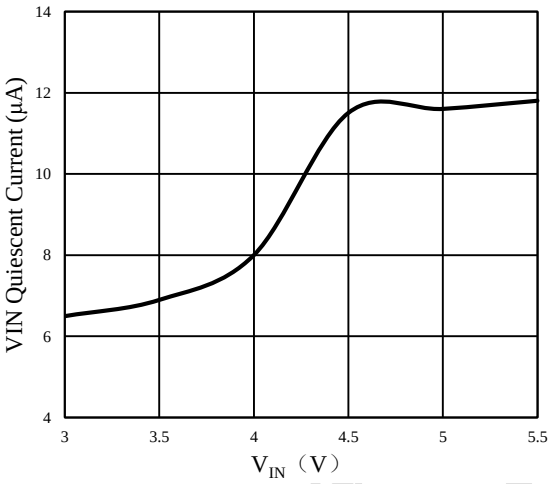


Figure 6. VIN Current vs. Input Voltage

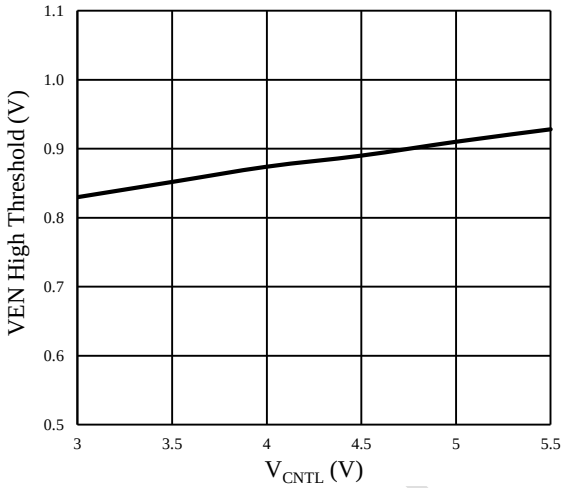


Figure 7. VEN_High vs Input Voltage

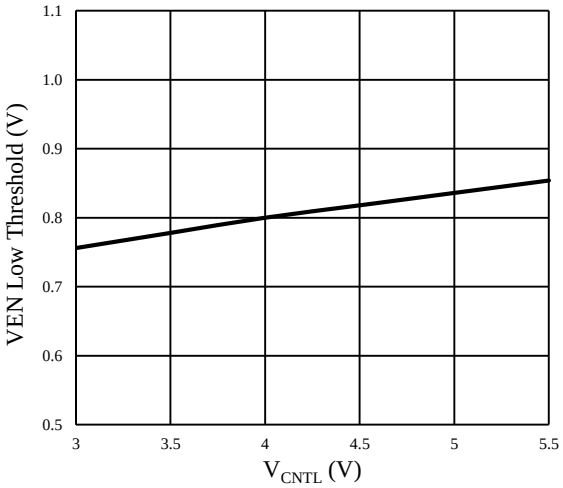


Figure 8. VEN_Low vs Input Voltage

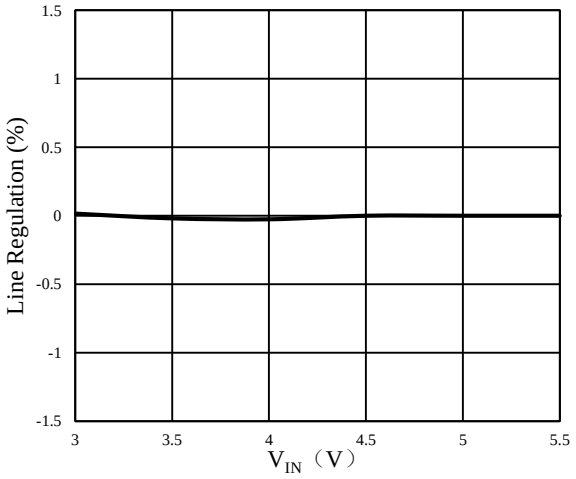


Figure 9 Line Regulation

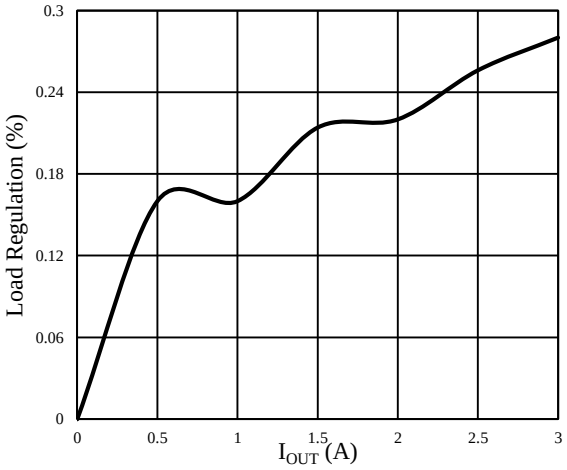


Figure 10 Load Regulation

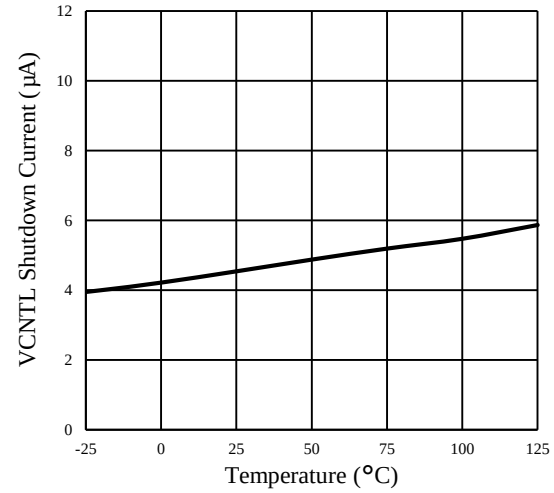


Figure 11 VCNTL Shutdown current vs. Temperature

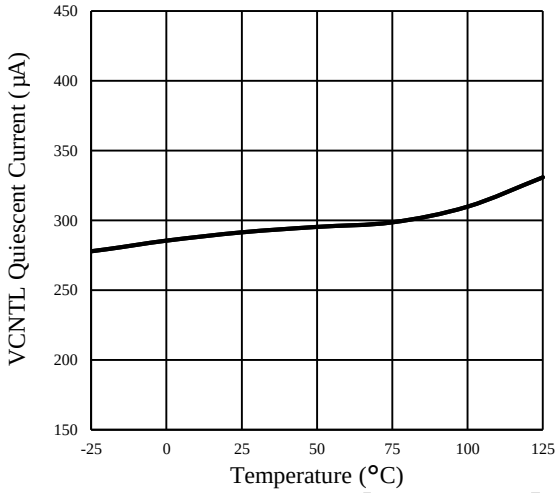


Figure 12 VCNTL Quiescent current vs. Temperature

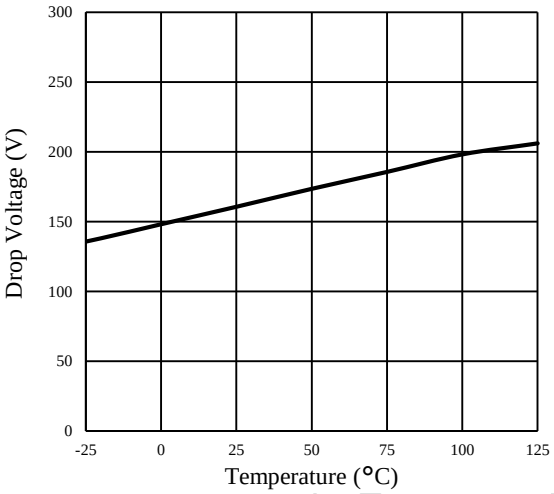


Figure 13 DROP Voltage vs. Temperature

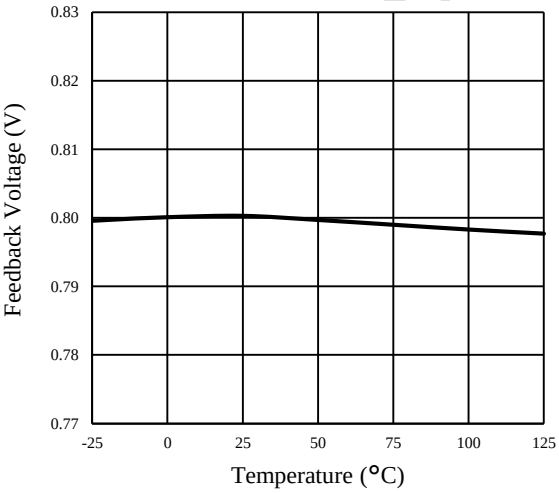


Figure 14 V_{FB} vs. Temperature

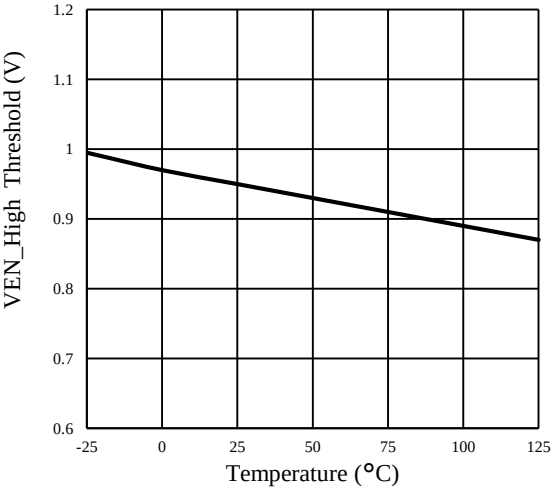


Figure 15 V_{EN}_High vs. Temperature

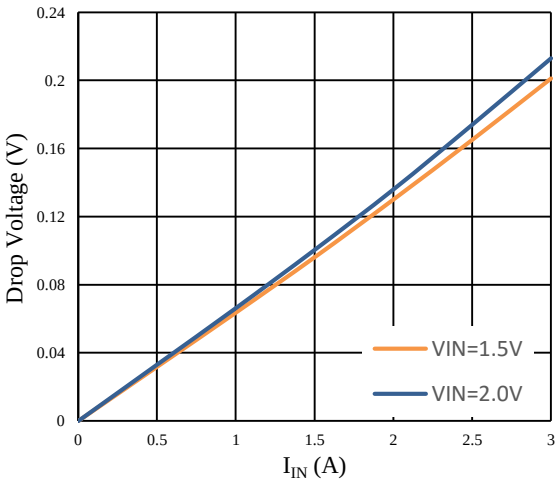


Figure 16 Drop Voltage vs. Load Current

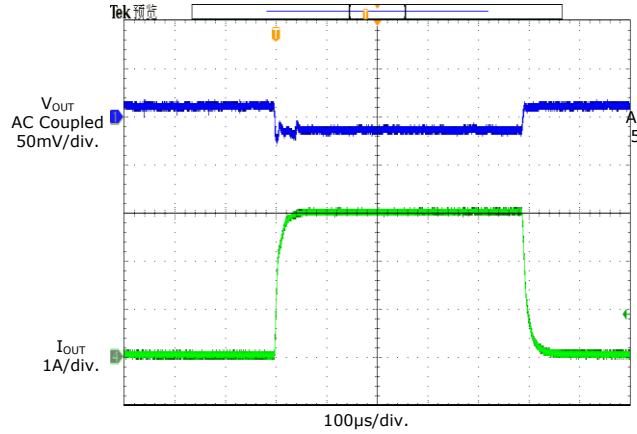


Figure 17 Load Transient
VOUT = 2.5V, IOUT =10mA to 3A

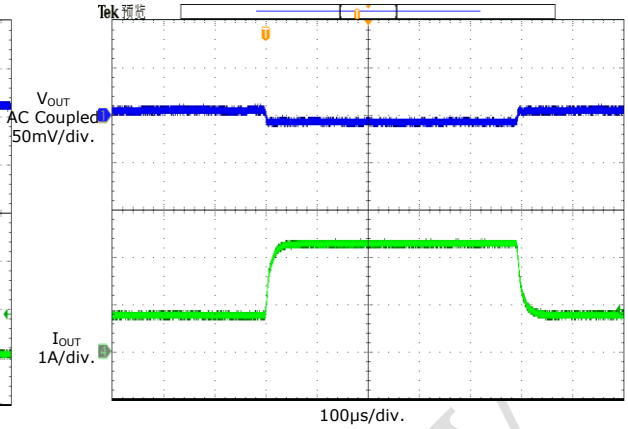


Figure 18 Load Transient
VOUT = 2.5V, IOUT =0.75A to 2.25A

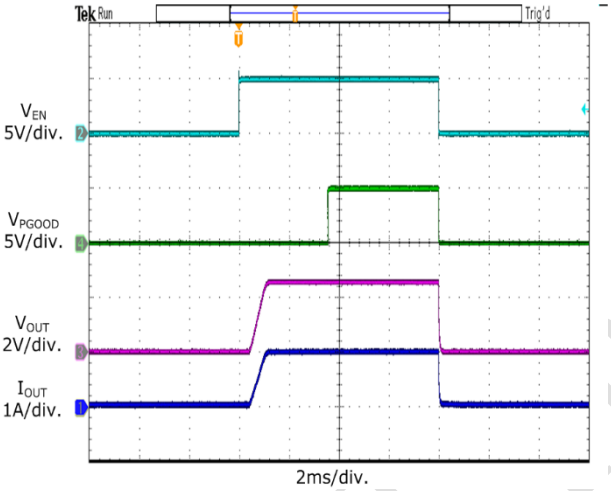


Figure 19 Power-Up Sequences

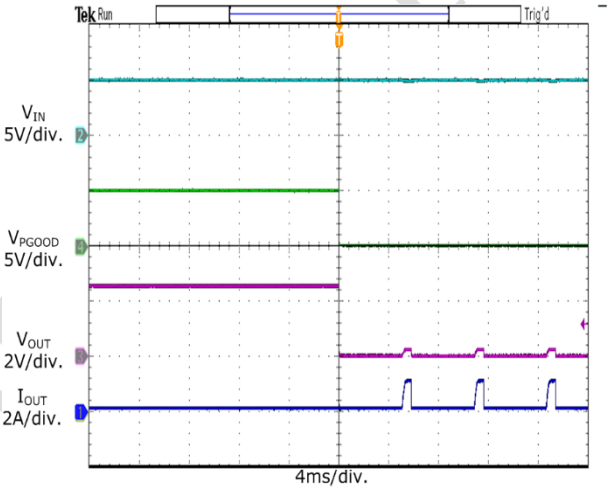


Figure 20 Output Short-Circuit Protection

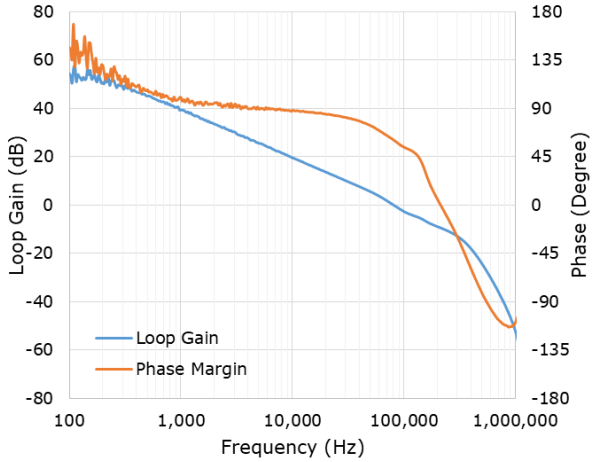


Figure 21 Phase and Gain vs. Frequency,
VOUT = 2.5V, IOUT = 20mA

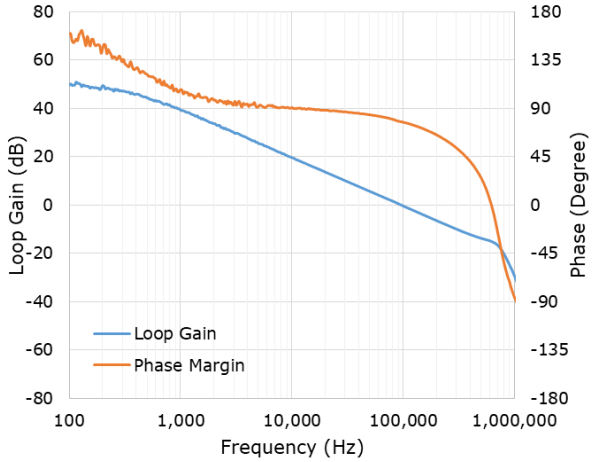
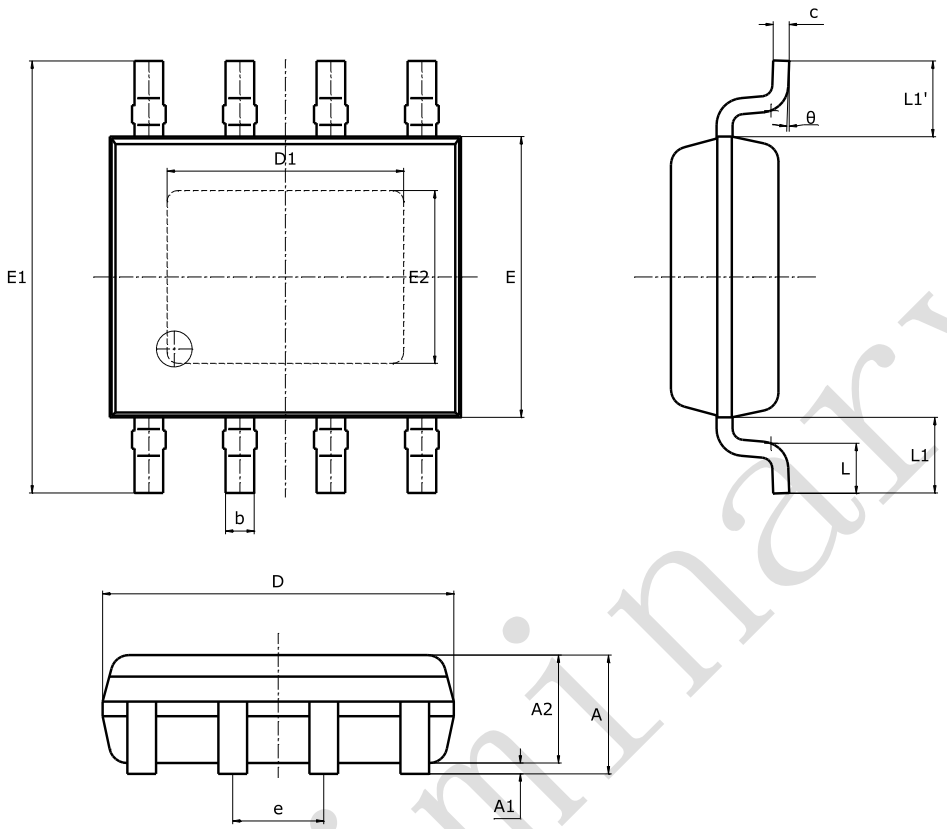


Figure 22 Phase and Gain vs. Frequency,
VOUT = 2.5V, IOUT = 2A

Package Information

SO8-EP Package Outline and Dimensions

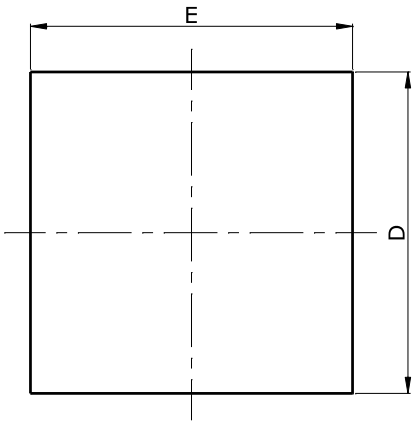


Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min.	Max.	Min.	Max.
A	1.400	1.700	0.055	0.067
A1	0.050	0.150	0.002	0.006
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.200
D1	3.202	3.402	0.126	0.134
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
E2	2.313	2.513	0.091	0.099
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
L1	1.04REF		0.041REF	
L1-L1’	—	0.12	—	0.005
θ	0º	8º	0º	8º

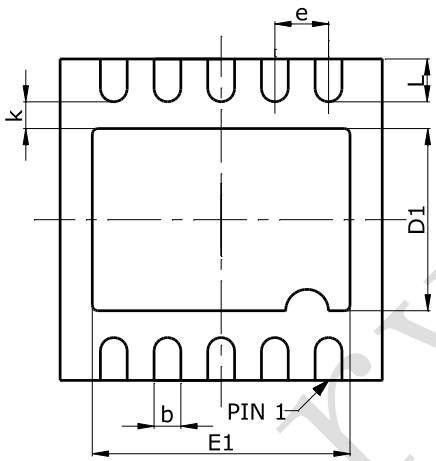
Notes:
1. This drawing is subjected to change without notice.
2. Body dimensions do not include mold flash or protrusion.
3. This package conforms to JEDEC MS-12, variation BA.

Package Information (continued)

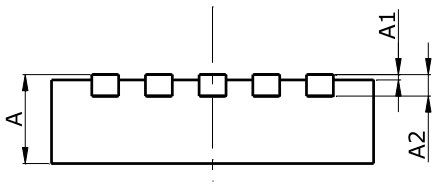
DFN-10 Package Outline and Dimensions



Top View



Bottom View

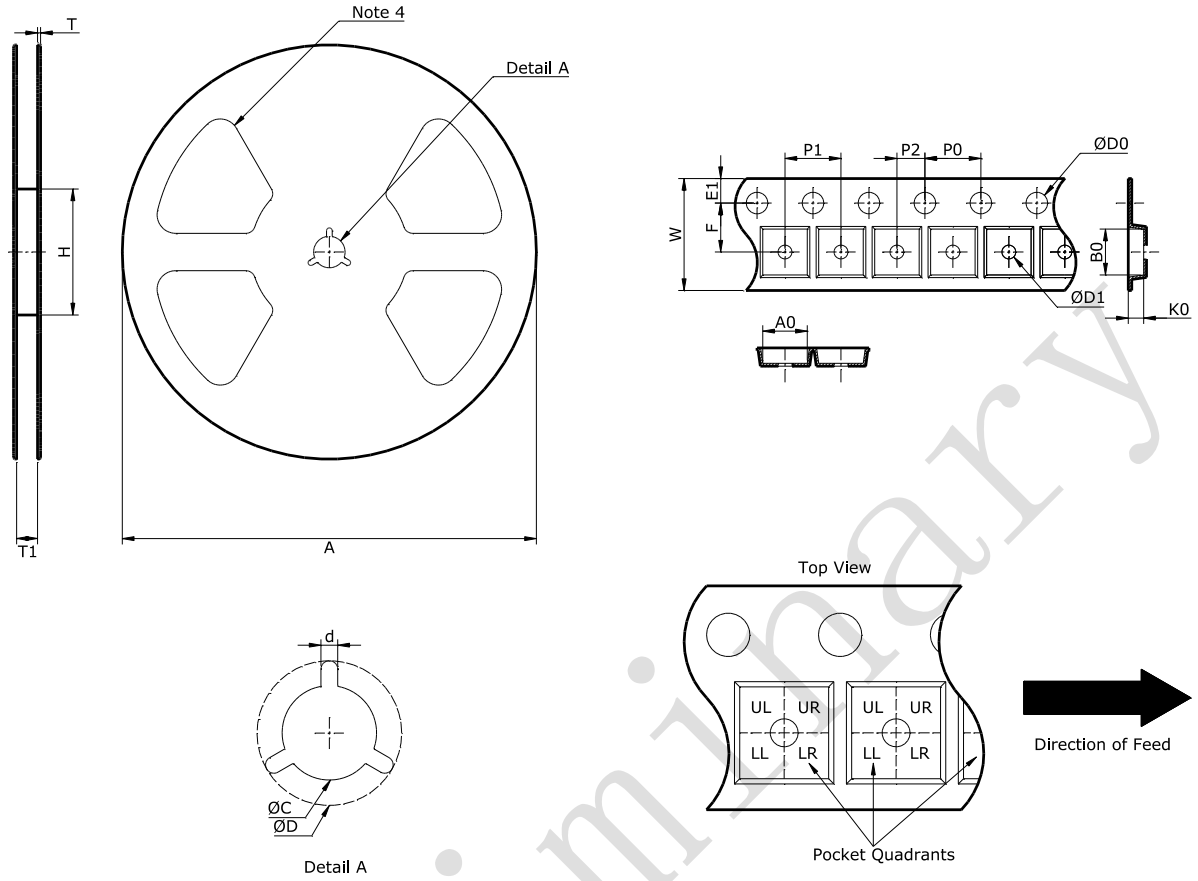


Side View

Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min.	Max.	Min.	Max.
A	0.700/0.800	0.800/0.900	0.028	0.031/0.035
A1	0.000	0.050	0.000	0.002
A2	0.153	0.253	0.006	0.010
D	2.900	3.100	0.114	0.122
E	2.900	3.100	0.114	0.122
D1	1.600	1.800	0.063	0.071
E1	2.300	2.500	0.091	0.098
k	0.200MIN.		0.008MIN.	
b	0.200	0.300	0.008	0.012
e	0.500TYP.		0.020TYP.	
L	0.300	0.500	0.012	0.020

Notes:
1. This drawing is subjected to change without notice.
2. Body dimensions do not include mold flash or protrusion.
3. This package conforms to JEDEC MO-187, variation AA.

Tape and Reel Information



DFN-10 Package									
A (mm)	**T (mm)**	**T1 (mm)**	**H (mm)**	**ØC (mm)**	**ØD (mm)**	**d (mm)**	**A0 (mm)**	**B0 (mm)**	**K0 (mm)**
330±1.0	2.6^{+1}_{-0}	12.4^{+1}_{-0}	100±0.5	13.0±0.2	17.70±0.40	1.9±0.4	3.35±0.1	3.35±0.1	1.13±0.1
W (mm)	**F (mm)**	**E1 (mm)**	**P0 (mm)**	**P1 (mm)**	**P2 (mm)**	**ØD0 (mm)**	**ØD1 (mm)**	**Pin 1 Quadrant**	
$12.00^{+0.3}_{-0.1}$	5.50±0.05	1.75±0.10	4.00±0.10	8.0±0.1	2.0±0.05	$1.5^{+0.10}_{-0}$	$1.5^{+0.25}_{-0}$	UL	
SO8-EP Package									
A (mm)	**T (mm)**	**T1 (mm)**	**H (mm)**	**ØC (mm)**	**ØD (mm)**	**d (mm)**	**A0 (mm)**	**B0 (mm)**	**K0 (mm)**
330±1.0	2.6^{+1}_{-0}	12.4^{+1}_{-0}	100±0.5	13.0±0.2	17.70±0.40	1.9±0.4	6.40±0.1	5.4±0.1	2.1±0.1
W (mm)	**F (mm)**	**E1 (mm)**	**P0 (mm)**	**P1 (mm)**	**P2 (mm)**	**ØD0 (mm)**	**ØD1 (mm)**	**Pin 1 Quadrant**	
$12.00^{+0.3}_{-0.1}$	5.50±0.1	1.75±0.10	4.00±0.10	8.0±0.1	2.0±0.05	$1.5^{+0.10}_{-0}$	$1.5^{+0.25}_{-0}$	UL	

Notes:
1. This drawing is subjected to change without notice.
2. All dimensions are nominal and in mm.
3. This drawing is not in scale and for reference only. Customer can contact Chipown sales representative for further details.
4. The number of flange openings depends on the reel size and assembly site. This drawing shows an example only.

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