CU6500/02VA(B) Family

Single PFC Controller
True-NoStandBy PFC for AC Adapter
OK with Stringent PC timing

Digital-Like PFC; EuP Lot 6 with PFC ON, Server Grade THD and PF; No need for special House Keeping

GENERAL DESCRIPTION

CU6500/02VA(B) family is Digital-Like single PFC controller and it is designed for EuP lot6 AC Adapter or True-NoStandBy PC Power. It has the following key features.

1.) True-NoStandby: Auxiliary Power is not necessary and it does not sacrifice the Stringent PC timing
2.) Power Consumption @ No Load (240W Power Supply) and @ Vin= 230Vac **~ 75mW and PFC is always on**
3.) Vcc Capacitor > 47uF // 0.1uF (high frequency one)
4.) Titanium Efficiency: Efficiency improved ~ 2% to 3% improved @ 50% load
5.) For ~ 100W to 2000W Power Supply Applications
6.) Turbo Speed PFC may reduce 420 Bulk Capacitor size further
7.) A PGB function is designed for interfacing to next stage controller or the House Keeping IC at secondary side. The PGB function pull low was decide by IC inside. The PGB Pull high when 380V boost output drops below ~ 295V at heavy load or when 380V drops below ~ 275V at light load
8.) 800V/18V UHV/BiCMOS Vanguard Process: 100 Ohm and 16V zener required at PFCOUT pin
9.) "Remember it was Light Load" function and "Remember it was Full Load" function may reduce PFC 420V Bulk Capacitor size further. It boosts the total efficiency as well.
10.) Initially, Vin at 230Vac, IC internal AC high line comparator determine is low line; therefore at light load, Bulk capacitor 380V can drop to 355V for CU6500/02VA(B).
11.) IAC: Rac is an exact external 7.0 Mega Ohm resistor
12.) CU6500/02VA SD pin: when 6V > SD > 2.5V with ~1.7mS delay, Power supply goes to "Retry" Mode; after Vcc < UVLOoff ~10.0V, it retries again.
13.) CU6500/02VA SD pin: when SD > 6.0V with ~1.7mS delay, Power Supply goes to "Latch" Mode; Vcc goes up and down between ~15.0V and ~12.0V until AC input removed and Vcc < UVLOoff ~10.0V, it retries again.
14.) CU6500/02VB SD pin: when SD > 2.5 with ~1.7mS delay, Power Supply goes to "Latch" Mode; Vcc goes up and down between ~15.0V and ~12.0V until AC power removed and Vcc < UVLOoff ~10.0V, it retries again.
15.) SD pin is designed for:
    A. OTP
    B. Bulk Redundant OVP
    C. Fault Summing Nodes such as OCP, OTP, or OVP from 6901V's Fault pin, or redundant external OVP
16.) Better Power Factor and THD ~ 5
17.) Clean Digital PFC Brown Out (On at ~80Vac and Off at ~65Vac)
18.) Dynamic Soft PFC to ease the stress over the entire external power device is reduced and EMI noise reduced
19.) Superior Surge Noise Immunity

CU6500/02VA(B) family(SLS IC at Secondary Side) is designed to meet the EPA/90+ regulation. With the proper design, its efficiency of power supply can reach Titanium Grade.

FEATURES

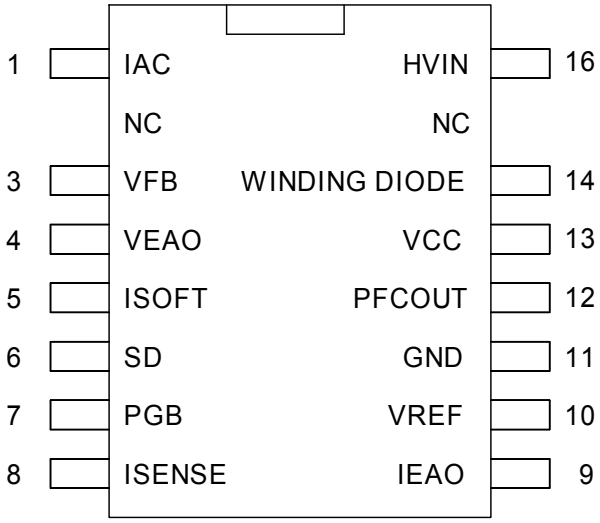
- Patents Pending
- Easy to design with
- 800V/18V UHV/Bi-CMOS Vanguard process. 100 Ohm and 16V zener required at PFCOUT (pin 12) and 16V zener required at Vcc (pin13)
- Designed to reach Titanium Grade with no Auxiliary Power
- Auxiliary Power is no long a necessary item: Efficiency Improved and Cost Reduced
- 3 voltage levels for PFC Boost Converter to ensure Stringent PC timing (410V (adjustable), 380V, 355V)
- 39V max input (WindingDiode pin14) LDO with Vcc Output ~ 15.3V
- Boost output dropped from 380V to 355V during light load for CU6502VA(B)
- No Need Vrms pin to sense input line condition anymore
- the Low Threshold ~ 295Vdc (heavy load) of PGB comparator at PGTHL internal node
- the Low Threshold ~ 275Vdc (light load) of PGB comparator at PGTHL internal node
- "Remember It was Light Load" function to improve the efficiency and Hold up Time
- "Remember It was Full Load" function to improve the efficiency and Hold up Time
- Initially, Vin at 230Vac, it is low line; therefore, at light load, Bulk 380V can drop to 355V
- Entering Kick Mode for Super Light Load when Po ~ 2%
- No Optical Current during Normal Operation for Super Light Load
- Clean Digital PFC Brown Out
- No extra bleed resistor: Internal Hefty Vanguard UHV Ultra-Fast Start Up
- Tstart-up < 100mS @ 90Vac with Cvcc = 200uF
- Long Sagging Delay Time ~ 0.5 S
- Dynamic Soft PFC to ease the stress of the Power Device and Ease the EMI-filter design.
- Better Power Factor and Better THD
- Average current mode control, continuous or discontinuous boost leading edge PFC
- Gain Modulator is a constant maximum power limiter
- In-Rush Current Protection
- Input OVP @ ~ 476Vdc
- Precision Current Limit, over-voltage protection, UVLO, and soft start, and Reference OK…
- Latch or Retry
- 16 Pin High Voltage Package
- CU6500/02VA for AC Adapter: when SD > 2.5V with 1.7mS, power supply goes to "Retry" Mode. When SD > 6.0V with 1.7mS, power supply goes to "Latch" Mode
- CU6500/02VB for Game Adapter/PC: when SD > 2.5V with 1.7mS, power supply goes to "Latch" Mode

APPLICATIONS

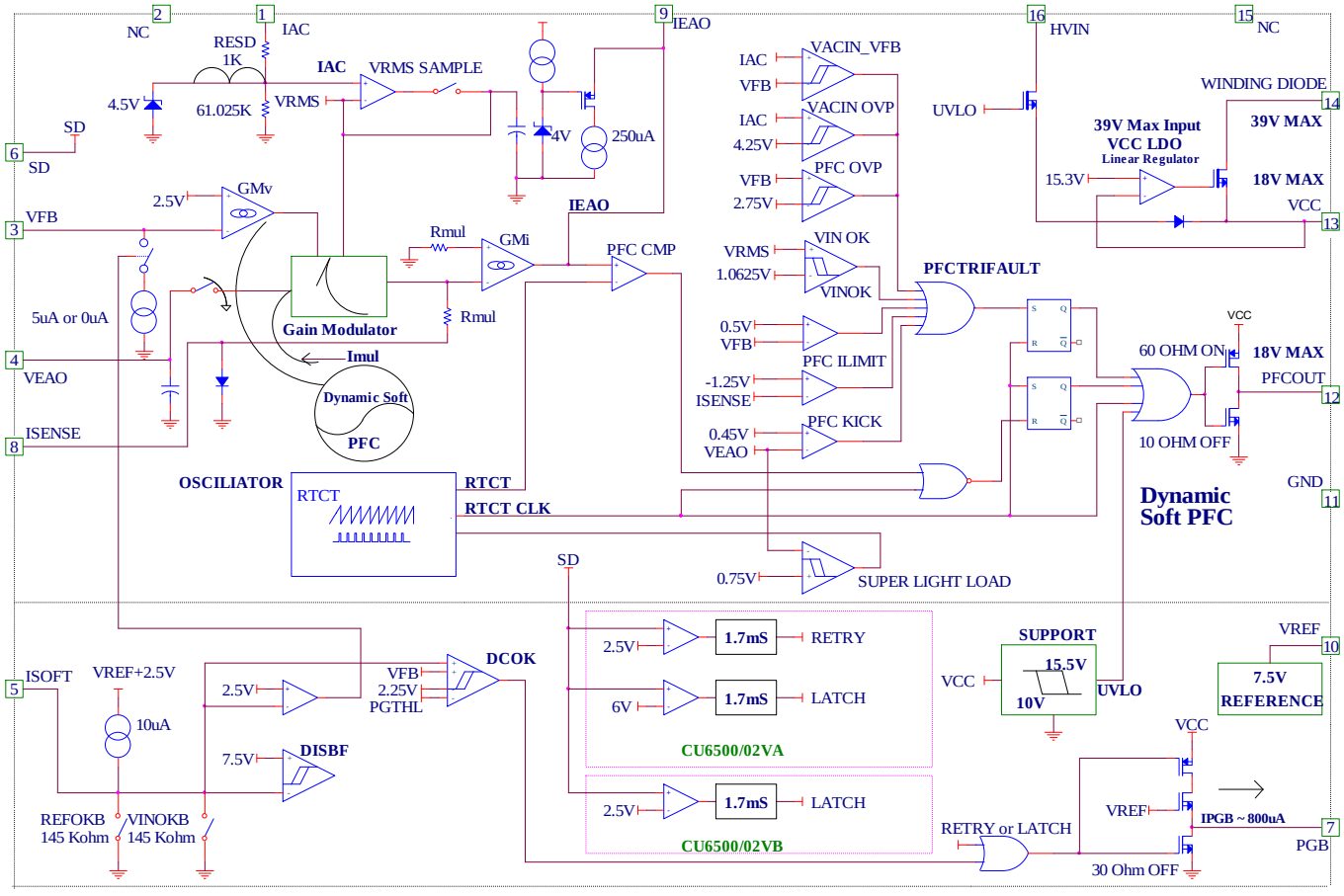
- EPA/90+ related Power Supply
- TV Power Supply
- Internet Server Power Supply: 200W to 2000W
- AC Adaptor for EuP lot6: 100W to 200W
- High Power LED for EuP lot6
- IPC Power Supply
- UPS
- Battery Charger
- DC Motor Power Supply
- Monitor Power Supply
- Telecom System Power Supply

PIN CONFIGURATION

SOP-16
TOP View



SIMPLIFIED BLOCK DIAGRAM



PIN DESCRIPTION

Pin No.	Symbol	Description	Operating Voltage			
			Min.	Typ.	Max.	Unit
1	I_{AC}	IAC has 2 functions: 1. PFC gain modulator reference input. 2. Need an external exact resistor, RAC = 7.0Mega Ohm to sense AC input after bridge diodes to generate SD voltage	0		5	V
2	NC	Pin2 has been removed for High Voltage Package				
3	VFB	PFC transconductance voltage error amplifier input	0	2.5	3	V
4	VEAO	PFC transconductance voltage error amplifier output (GMv)	0		6	V
5	ISOFT		0		Vcc	V
6	SD	**CU6500/02VA (for AC Adapter) : SD** > 2.5V w ~1.7mS timer delay →Retry Mode and SD > 6.0V ~ 1.7mS timer delay →Latch Mode **CU6500/02VB (for Gaming or PC): SD** > 2.5V w ~1.7mS timer delay → Latch Mode	0		7.5	V
7	PGB	PGB is the PG comparator output. The input of PG comparator is using VFB (pin3) to compare with the high threshold 2.25V (after ISOFT>7.5V, Bulk~342Vdc) and the low threshold comparator with PGTHL ~ 1.94V (after ISOFT>7.5V, Bulk~295Vdc) at Heavy Load and PGTHL ~ 1.81V (after ISOFT>7.5V, Bulk~275Vdc) at Light Load. When Bulk Voltage 380V is ready, pin 7 is pulled to 0V. When Bulk Voltage Drop (VFB (PIN3)<PGTHL) below internal set point it will be pulled high and it will light up Optical Couple to turn off SLS Controller, CU6901V at Secondary Side.	0		VCC	V
8	ISENSE	PFC Current Sense: for both Gain Modulator and PFC current ILIMIT comparator.	-1.3		0.7	V
9	IEAO	PFC transconductance current error amplifier output **(GMi).**	0	2.5	8	V
10	VREF	Maximum 3.5mA buffered output for the internal 7.5V reference when VCC=14V		7.5		V
11	GND	Ground				
12	PFCOUT	PFC CMOS Gate driver output	0		VCC	V
13	V_{CC}	Positive supply for CU6500/02VA(B); usually, it is regulated by internal 39V LDO with 15.3V output if Winding Diode pin > 20V	10	15.3	18	V
14	WINDING DIODE	Internal WindingDiode-Vcc LDO input to tap Main Transformer Energy. Maximum input ~ 39V with regulated output ~ 15.3V. The typical Winding Diode pin ~ 20V	0		39	V
15	NC	Pin15 has been removed for High Voltage Package				
16	HVIN	HVIN needs an external current limit resistor, 20Kohm to take energy from after Bridge-Diodes Node	0		600	V

ORDERING INFORMATION

Part Number	Temperature Range	Package
CU6500VAISTR*	-40℃ to 125℃	16-Pin SOP (S16)
CU6500VBISTR*	-40℃ to 125℃	16-Pin SOP (S16)
CU6502VAISTR*	-40℃ to 125℃	16-Pin SOP (S16)
CU6502VBISTR*	-40℃ to 125℃	16-Pin SOP (S16)

***Note:** TR : Package is Tape & Reel

Part Number Descrption	VFB Current for ISOFT < 2.5V	O.T.P/Redundant BulkOVP
CU6500/02VA	5uA	Retry (SD>2.5V with 1.7mS timer) / Latch (SD>6V with 1.7mS timer)
CU6500/02VB	5uA	Latch (SD>2.5V with 1.7mS timer)

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum ratings are those values beyond which the device could be permanently damaged.

Parameter	Min.	Max.	Units
HVIN (pin16)	GND	800	V
HVIN (pin16) Less than 10uS with 1mA maximum	GND	600	V
HVIN (pin16) Less than 1mS with 20mA maximum	GND	400V	V
HVIN (pin16) continuous DC 0.8mA maximum	GND	400V	V
HVIN (pin16) external series resistor to after-bridge-diodes node	20K		Ohm
V_{CC} (pin13)		18	V
39V WindingDiode (pin14)	0	39	V
39V WindingDiode (pin14) continuous DC Sinking Current	0	10	mA
VREF (pin10)	GND – 0.3	8	V
VREF (pin10) (forced externally) (period less than 1ms)		8.5	V
VREF (pin10) (forced externally) overshoot (period less than 300us)		10	V
IEAO (pin9) / VEAO (pin4) / SD (pin6)	GND – 0.3	10	V

Parameter	Min.	Max.	Units
IAC (pin1)	GND – 0.3	6	V
PGB (pin7)	GND – 0.3	6	V
PGB (pin7) when PGB pulled high from internal logic; external Rpgb	0.5K		Ohm
PGB (pin7): PGB current will increase the stress at HVIN (pin16)		0.7	mA
ISOFT (pin5)	GND – 0.3	VCC+0.7	V
VFB (pin3)	GND – 0.3	5	V
ISENSE (pin8) Voltage	-5	0.7	V
ISENSE (pin8) Voltage (period less than 1ms)	-10	0.7	V
PFC OUT (pin12)	GND – 0.3	VCC + 0.3	V
PFC Out (pin12) Driver (period less than 50ns)	GND – 3.0	VCC + 0.3	V
PFC Out (pin12) Driver (period less than 25ns)	GND – 5.0	VCC + 0.3	V
Peak PFC OUT (pin12) Current, Source or Sink		0.5	A
Peak PFC OUT (pin12) Current, Source or Sink (period less than 5us)		1	A
PFC OUT (pin12), Energy Per Cycle		1.5	μJ
I_{REF} (pin10)		3.5	mA
I_{AC} (pin1)		6	V
Junction Temperature		150	℃
Storage Temperature Range	-65	150	℃
Operating Temperature Range	-40	125	℃
Lead Temperature (Soldering, 10 sec)		260	℃
Thermal Resistance (θ_{JA}) / Plastic SOP		105	℃/W
Case Temperature (θ_{JC}) / Plastic SOP		31.25	℃/W

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, these specifications apply Vcc (pin13) ~ +15.3V, WindingDiode (pin14) = 20V, T_A=Operating Temperature Range Room Temperature=25℃ (Note 1)

Symbol	Parameter	Test Conditions	CU6500/02VA(B) Family			Unit
			Min.	Typ.	Max.	
Clean Digital PFC Brown in/Out						
Brown In	On Threshold High		1.02	1.05	1.08	V
Brown Out	Off Threshold Low after AC clock timer (~0.5S)		0.91	0.95	0.99	V
	Hysteresis			100		mV
Latch Mode or Retry Mode						
SD (pin6) for CU6500/02VA	OTP/Redundant Bulk OVP	2ms 2.7V Pulse if it goes to Retry Mode	2.4	2.5	2.6	V
SD (pin6) for CU6500/02VA	OTP/Redundant Bulk OVP	2ms 7.0V Pulse if it goes to Latch Mode	5.5	6.0	6.5	V
SD (pin6) for CU6500/02VB	OTP/Redundant Bulk OVP	2ms 2.5 Pulse if it goes to Latch Mode	2.4	2.5	2.6	V
SD (pin6) for CU6500/02VA (B)	OTP/Redundant Bulk OVP (Note 4)	0.5ms 2.7V/7.0V Pulse if it goes to Latch Mode		1.7		mS
Voltage Error Amplifier (GMv) VEAO (PIN4)						
	Input Voltage Range		0		6	V
	Transconductance	V_{NONINV} = V_{INV}, VEAO (PIN4) = 2.25V	40	50	60	μmho
VFB(pin3) (high) Full load	Feedback Reference Voltage (High)	Vrms > AC High Line Threshold VEAO (pin4) > 2.25V and Vrms < AC high Line Threshold	2.48	2.5	2.52	V
CU6500/02VA(B) Family						
VFB Current	Feedback Reference current	Vcc=16v, ISOFT=1.5v, VFB=4.5v		5		uA
Light/Full Load determine (VEAO (pin4) Threshold)						
VEAO (pin4)	Full Load Threshold	VFB (PIN3)=Feedback Reference Voltage (High)	2.24	2.375	2.49	V
VEAO (pin4)	Light Load Threshold	VFB (PIN3)=Feedback Reference Voltage (Low)	1.66	1.75	1.84	V
	Hysteresis		580	625	650	mV
	Output High Voltage	VFB = 2.0V after ISOFT > 7.5V	5.3	5.5		V
	Output Low Voltage	VFB = 2.6V		5	20	mV
	Source Current	Overdrive Voltage = 100mV	2	4	6	μA
	Sink Current	Overdrive Voltage = 100mV	-65		-45	μA
	Open Loop Gain	DC gain	30	40		dB
	Power Supply Rejection Ratio	11V < V_{CC} < 16.5V	60	75		dB

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, these specifications apply Vcc (pin13) ~ +15.3V, WindingDiode (pin14) = 20V, T_A=Operating Temperature Range Room Temperature=25℃ (Note 1)

Symbol	Parameter	Test Conditions	CU6500/02VA(B) Family			Unit
			Min.	Typ.	Max.	
Current Error Amplifier (GMi) IEAO (pin9)						
	Transconductance	V_{NONINV} = V_{INV}, IEAO (pin9) = 2.5V	10	20	30	μmho
	Input Referred Offset Voltage	VEAO (pin4)=0.6V, IAC is open	-20		-15	mV
	Output High Voltage		4.3	4.8	5.3	V
	Output Low Voltage			5	20	mV
	Sink Current	ISENSE (pin8) = -0.5V, IEAO (pin9) = 1.5V	-60	-50	-40	μA
	Source Current	ISENSE (pin8) = +0.5V, IEAO (pin9) = 4.0V	40	50	60	μA
	Open Loop Gain	DC Gain	30	40		dB
	Power Supply Rejection Ratio	11V < V_{CC} < 16.5V	60	75		dB
PFC OVP Comparator						
	Threshold Voltage		2.63	2.72	2.8	V
	Hysteresis		140		240	mV
PFC Kick Comparator						
	VEAO (pin4) Threshold Voltage		0.47	0.5	0.53	V
Tri-Fault Detect						
	Fault Detect HIGH		2.63	2.72	2.8	V
	Time to Fault Detect HIGH	VFB (pin3)=$V_{FAULT\ DETECT\ LOW}$ to VFB (pin3)=OPEN, 470pF from VFB (pin3) to GND		2	4	ms
	Fault Detect LOW		0.47	0.5	0.53	V
PFC I_{LIMIT} Comparator(PFC current limit)						
	Threshold Voltage		-1.32	-1.25	-1.12	V
	(PFCI_{LIMIT}– Gain Modulator $Output_{max}$)		300	450		mV
	Delay to Output (Note 4)			700		ns

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, these specifications apply Vcc (pin13) ~ +15.3V, WindingDiode (pin14) = 20V, T_A=Operating Temperature Range Room Temperature=25℃ (Note 1)

Symbol	Parameter	Test Conditions	CU6500/02VA(B) Family			Unit
			Min.	Typ.	Max.	
PGBTH: PGB threshold (Sensing VFB (pin3) determines to pull high or pull low PGB pin)						
PGBTHH	PGB_CMP_LOW	Sweep VFB (pin3) than check PGB (pin7) pull low	2.18	2.25	2.31	V
PGBTHL for VEAO > 2.25V CU6500/02VA	PGB_CMP_HIGH	Sweep VFB (pin3) than check PGB (pin7) pull high	1.7	1.74	1.78	V
VA Hysteresis	Remember (Full Load) – (Light Load) Hysteresis	Sweep VFB (pin3) than check PGB (pin7) pull high		60	90	mV
PGBTHL for VEAO > 2.25V CU6500/02VB	PGB_CMP_HIGH	Sweep VFB (pin3) than check PGB (pin7) pull high	1.92	1.95	1.98	V
VB Hysteresis	Remember (Full Load) – (Light Load) Hysteresis	Sweep VFB (pin3) than check PGB (pin7) pull high		60	90	mV
GAIN Modulator						
	Imul x Rmul (IAC=1.443V)	I_{AC} (pin1) = 1.443V (Line=115Vac), VEAO (pin4) = 2.25V		390		mV
	Imul x Rmul (IAC=2.898V)	I_{AC} (pin1) = 2.898V (Line=230Vac), VEAO (pin4) = 2.25V		185		mV
	Imul x Rmul (IAC=3.328V)	I_{AC} (pin1) = 3.328V (Line=264Vac) , VEAO (pin4) = 2.25V		160		mV
	Bandwidth (Note 4)	I_{AC} (pin1) = 1.126V (Line=90Vac)		1		MHz
Oscillator (Measuring fpfc)						
	Initial fpfc Accuracy 1	R_T = 27 kΩ, C_T = 1000pF, IAC=1.126V	64	67.5	71	kHz
	Voltage Stability	11V < V_{CC} < 16.5V		2		%
	Temperature Stability			2		%
	Ramp Valley to Peak Voltage	VEAO (pin4)=5.5V and IAC (pin1) =20uA; Sweep IEAO (pin9)		2.5		V
	PFC Dead Time (Note 4)	IEAO (pin9)=1.0V; measure the PFC off time		457		ns
	Fpfc @ Super Light Load	Veao < 0.75V	23	26	29	KHz

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, these specifications apply Vcc (pin13) ~ +15.3V, WindingDiode (pin14) = 20V T_A=Operating Temperature Range Room Temperature=25℃ (Note 1)

Symbol	Parameter	Test Conditions	CU6500/02VA(B) Family			Unit
			Min.	Typ.	Max.	
Reference						
	Output Voltage	I(VREF) = 0mA	7.48	7.52	7.56	V
	Line Regulation	11V < V_{CC} < 16.5V		95	150	mV
	Load Regulation	VCC=10.5V,0mA < I(VREF) < 2.0mA ; @ T=25℃		15	30	mV
		VCC=14V,0mA < I(VREF) < 3.5mA ; T_A = -40℃~125℃		15	30	mV
	Temperature Stability			0.4		%
	Total Variation	Line, Load, Temp	7.3		7.7	V
	Long Term Stability	T_J = 125℃, 1000HRs	5		25	mV
PFCOUT (pin12)						
	Minimum Duty Cycle	$V_{IEAO\ (PIN9)}$ > 4.0V		0		%
	Maximum Duty Cycle	$V_{IEAO\ (PIN9)}$ < 1.2V	93	95		%
	Output Low Rdson	I_{OUT} = -20mA		12	18	ohm
		I_{OUT} = -100mA			18	ohm
		I_{OUT} = 10mA, V_{CC} = 9V		0.5	1	V
	Output High Rdson	I_{OUT} = 20mA		20	30	ohm
		I_{OUT} = 100mA			30	ohm
	Rise/Fall Time (Note 4)	C_L = 100pF		50		ns
ISOFT (pin5)						
	Soft Start Current		8	10	12	μA
Vcc (pin13)						
	Start-Up Current	V_{CC} = 14V, C_L = 0		50	75	uA
	Operating Current	15.3V, C_L = 0		1	1.2	mA
$UVLO_{on}$	Under voltage Lockout Threshold		14.7	15.5	16.3	V
$UVLO_{on}$ - $UVLO_{off}$	Under voltage Lockout Hysteresis			5		V
39V WindingDiode-Vcc LDO, WindingDiode (pin14)						
	Vcc, WindingDiode-Vcc LDO output voltage	WindingDiode (pin14) = 20V	14.53	15.3	16.1	V
	Vcc, WindingDiode-Vcc LDO output current	WindingDiode (pin 14)= 20V and Vcc = 14V		30		mA
HVIN (maximum 600V operation) (pin16)						
	HVIN (pin16) Current at Vcc = 15V	HVIN (pin16) =40V; Vcc (pin13) = 15V		2		mA
	HVIN (pin16) Current at Vcc = 11V	HVIN (pin16) =40V; Vcc (pin13) = 11V		6		mA
	HVIN (pin16) Current at Vcc = 0V	HVIN (pin16) =40V; Vcc (pin13)= 0V		30		mA
IHVIN leakage	HVIN (pin16) Leakage Current	HVIN (pin16) =800V; Vcc (pin13) = 15.3V			1	uA
BV HVIN (pin16)	HVIN Off Break Down Voltage	Sweep HVIN (pin16) ; Vcc (pin13) = 15.3V (Note: 5)			800	V

Note 1: Limits are guaranteed by 100% testing, sampling, or correlation with worst-case test conditions.
Note 2: Includes all bias currents to other circuits connected to the VFB (pin3) pin.
Note 3: Gain ~ K x 5V; K = (ISENSE (pin8) – I_{OFFSET}) x $[I_{AC}$ (VEAO (pin4) – 0.5)$]^{-1}$; VEAO $(pin4)_{MAX}$ = 5.5V
Note 4: Guaranteed by design, not 100% production test
Note 5: Characterization only and sample test only, not test at production

Getting Start

To start evaluating CU6500/02VA(B) from the exiting CM6502 , need to be taken care before doing the fine tune:

1.) Remove Stand By Auxiliary Power Supply and related circuit
2.) IAC (pin1) needs an exact external resistor, 7Mega ohm to sense the input AC signal after bridge diode
3.) SD pin (pin6): CU6500/02VA for AC Adapter and CU6500/02VB for Gaming and PC "True-NoStandBy"
   - CU6500/02VA: SD>2.5V with ~ 1.7mS goes to Retry Mode; Power Supply Off until Vcc < UVLOoff = 10.0V, Power Supply retries again
   - CU6500/02VA: SD>6.0V with ~ 1.7mS goes to Latch Mode; Power Supply Off and Vcc goes up and down between 15V and 12V; until AC removed and Vcc < UVLOoff = 10.0V, Power Supply retries again
   - CU6500/02VB: SD>2.5V with ~ 1.7mS goes to Latch Mode; Power Supply Off and Vcc goes up and down between 15V and 12V; until AC removed and Vcc < UVLOoff = 10.0V, Power Supply retries again
4.) Connect HVIN (pin16) in series with 20K ohm current limit resistor to tap the energy after Bridge Diodes and there is an internal 800V UHV Start Up Circuit on/off when it is necessary
5.) To have the optimal efficiency and timing performance, use the maximum 39V WindingDiode (pin14) input LDO to take the energy from main transformer energy. WindingDiode (pin14) is the 39V max LDO input and the 39V LDO output is Vcc pin. Vcc is regulated ~ 15.3V when WindingDiode (pin14) = 20V. Please set WindingDiode < 20 at steady state for the optimal efficiency and timing.
6.) Vcc Bypass Capacitor > 47uF // with a high frequency MLCC capacitor such as 0.1uF; it provide the optimal timing and efficiency performance
7.) Protect Vcc (pin13) and PFC (pin12): CU6500/02VA(B) using Vanguard 800V/18V UHV/BCD process; since the low voltage section is an 18V process, PFCOUT (pin12) and Vcc (pin13), each pin requires an external 16V zeners to GND to protect back **EMF** energy from the external circuit. Also, PFCOUT needs 10 ohm in series before connecting an external totem pole circuit
8.) Protect ISENSE (pin8): ISENSE (pin8) has a negative ESD (SCR) and it is sensitive to high dV/dt. Try to slow down the ISENSE (pin8) dV/dt. Beside a good inrush current protection circuit for PFC Boost is recommended, a 3 diodes in series at ISENSE (pin8) is needed since the PFCILIMIT threshold ~ -1.25V

Functional Description

CU6500/02VA(B) is designed for high efficient power supply for both full load and light load. It is a Digital-Like PFC supply controller and it is designed to have the better performance than Digital PFC. Its THD ~ 5 at Full Load @ 230Vac.

The CU6500/02VA(B) is an average current controlled, continuous/discontinuous boost Power Factor Correction (PFC) which uses leading edge modulation.

Power Factor Correction In general

Power factor correction makes a nonlinear load look like a resistive load to the AC line. For a resistor, the current drawn from the line is in phase with and proportional to the line voltage, so the power factor is unity (one). A common class of nonlinear load is the input of most power supplies, which use a bridge rectifier and capacitive input filter fed from the line. The peak-charging effect, which occurs on the input filter capacitor in these supplies, causes brief high-amplitude pulses of current to flow from the power line, rather than a sinusoidal current in phase with the line voltage. Such supplies present a power factor to the line of less than one (i.e. they cause significant current harmonics of the power line frequency to appear at their input). If the input current drawn by such a supply (or any other nonlinear load) can be made to follow the input voltage in instantaneous amplitude, it will appear resistive to the AC line and a unity power factor will be achieved.

To hold the input current draw of a device drawing power from the AC line in phase with and proportional to the input voltage, a way must be found to prevent that device from loading the line except in proportion to the instantaneous line voltage. The PFC section of the CU6500/02VA(B) uses a boost-mode AC-DC converter to accomplish this. The input to the converter is the full wave rectified AC line voltage. No bulk filtering is applied following the bridge rectifier, so the input voltage to the boost converter ranges (at twice line frequency) from zero volts to the peak value of the AC input and back to zero. By forcing the boost converter to meet two simultaneous conditions, it is possible to ensure that the current drawn from the power line is proportional to the input line voltage. One of these conditions is that the output voltage of the boost converter must be set higher than the peak value of the line voltage. A commonly used value is 385VDC, to allow for a high line of $270VAC_{rms}$. The other condition is that the current drawn from the line at any given instant must be proportional to the line voltage. Establishing a suitable voltage control loop for the converter, which in turn drives a current error amplifier and switching output driver satisfies the first of these requirements. The second requirement is met by using the rectified AC line voltage to modulate the output of the voltage control loop. Such modulation causes the current error amplifier to command a power stage current that varies directly with the input voltage. In order to prevent ripple, which will necessarily appear at the output of boost circuit (typically about 10VAC on a 385V DC level); from introducing distortion back through the voltage error amplifier, the bandwidth of the voltage loop is deliberately kept low. A final refinement is to adjust the overall gain of the PFC such to be proportional to 1/(Vin x Vin), which linearizes the transfer function of the system as the AC input to voltage varies.

Since the boost converter topology in the CU6500/02VA(B) PFC is of the current-averaging type, no slope compensation is required.

More exactly, the output current of the gain modulator is given by:

In addition to power factor correction, a number of protection features have been built into the CU6500/02VA(B). These include PFC input OVP, soft-start, PFC over-voltage protection, peak current limiting, In-Rush Current protection, brownout protection, duty cycle limiting, and under-voltage lockout.

Digital-Like PFC (Patent Pending)

Digital-Like PFC feature is designed to replace Digital PFC. The current THD ~ 5 at 50% Load @ Vin = 230Vac.

Dynamic Soft PFC

Dynamic Soft PFC is the main feature of CU6500/02VA(B). Dynamic Soft PFC is to improve the efficiency, to reduce power device stress, to ease EMI, and to ease the monotonic output design while it has the more protection such as the short circuit with power-fold-back protection. Its unique sequential control maximizes the performance and the protections among steady state, transient and the power on/off conditions.

PFC Main Control Section

Gain Modulator

Vrms pin is no longer needed and digital-like PFC is implemented to improve THD and Line Transient Response.

CU6500/02VA(B) gain modulator is the heart of the PFC, as it is this circuit block which controls the response of the current loop to line voltage waveform and frequency, rms line voltage, and PFC output voltages. There are three inputs to the gain modulator. These are:

1. A current representing the instantaneous input voltage (amplitude and wave-shape) to the PFC. The rectified AC input sine wave is converted to a proportional current via a resistor and is then fed into the gain modulator at I_{AC}. Sampling current in this way minimizes ground noise, as is required in high power switching power conversion environments. The gain modulator responds linearly to this current.
2. A voltage proportional to the long-term RMS AC line voltage, derived from the rectified line voltage after scaling and filtering. This signal is presented to the gain modulator at SD (pin6). The gain modulator's output is inversely proportional to $Vrms^2$. The relationship between Vrms and gain is illustrated in the Typical Performance Characteristics of this page but Vrms pin is no longer needed.
3. The output of the voltage error amplifier, VEAO (pin4). The gain modulator responds linearly to variations in this voltage.

The output of the gain modulator is a current signal, in the form of a full wave rectified sinusoid at twice the line frequency. This current is applied to the virtual-ground (negative) input of the current error amplifier. In this way the gain modulator forms the reference for the current error loop, and ultimately controls the instantaneous current draw of the PFC from the power line. The general formula of the output of the gain modulator is:

$$I_{mul} = \frac{I_{AC} \times (VEAO - 0.5V)}{V_{RMS}^2} \text{ x constant} \qquad (1)$$

Gain=Imul/Iac

K=Gain/(VEAO (PIN4)-0.5V)

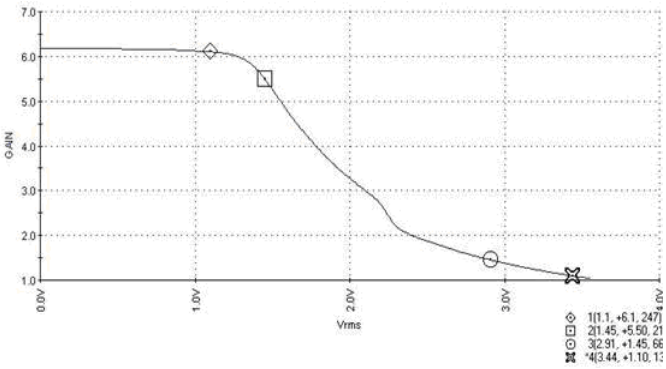
$I_{mul} = K \times (VEAO\ (PIN4) - 0.5V) \times I_{AC}$

Where K is in units of $[V^{-1}]$

Note that the output current of the gain modulator is limited around 80uA and the maximum output voltage of the gain modulator is limited to 80uA x 10K = 0.8V. This 0.8V also will determine the maximum input power.

However, $I_{GAINMOD}$ cannot be measured directly from ISENSE (pin8). ISENSE (pin8) = $I_{GAINMOD}$-I_{OFFSET} and I_{OFFSET} can only be measured when VEAO (pin4) is less than 0.5V and $I_{GAINMOD}$ is ~ 0A. Typical I_{OFFSET} is around 7.8uA.

VEAO (PIN4)=5.5V



Gain vs. SD (pin6)

When SD below 1V, the PFC is shut off. Designer needs to design 80VAC with SD average voltage= 1.0V.

$$\text{Gain} = \frac{I_{SENSE} - I_{OFFSET}}{I_{AC}} = \frac{I_{MUL}}{I_{AC}}$$

The external R_{AC} = 7.0 Mega Ohm for IAC (pin1)

IAC (pin1) is the input of the gain modulator. The external R_{AC}=7.0 Mega Ohm, it will provide a good sine wave current derived from the line voltage and it also helps program the maximum input power and minimum input line voltage.

R_{AC}=Vin min peak x 61.88K. For example, if the minimum line voltage is 80VAC, the R_{AC}=80 x 1.414 x 61.88K = 7.0 Mega ohm.

SD (pin6) Description

CU6500/02VA is for AC Adapter and CU6500/02VB is for Gaming and PC "True-NoStandBy"

- CU6500/02VA: SD>2.5V with ~ 1.7mS goes to Retry Mode; Power Supply Off until Vcc < UVLOoff = 10.0V, Power Supply retries again
- CU6500/02VA: SD>6.0V with ~ 1.7mS goes to Latch Mode; Power Supply Off and Vcc goes up and down between 15V and 12V; until AC removed and Vcc < UVLOoff = 10.0V, Power Supply retries again
- CU6500/02VB: SD>2.5V with ~ 1.7mS goes to Latch Mode; Power Supply Off and Vcc goes up and down between 15V and 12V; until AC removed and Vcc < UVLOoff = 10.0V, Power Supply retries again

Current Error Amplifier, IEAO (pin9)

The current error amplifier's output controls the PFC duty cycle to keep the average current through the boost inductor a linear function of the line voltage. At the inverting input to the current error amplifier, the output current of the gain modulator is summed with a current which results from a negative voltage being impressed upon the ISENSE (pin8). The negative voltage on ISENSE (pin8) represents the sum of all currents flowing in the PFC circuit, and is typically derived from a current sense resistor in series with the negative terminal of the input bridge rectifier.

In higher power applications, two current transformers are sometimes used, one to monitor the IF of the boost diode. As stated above, the inverting input of the current error amplifier is a virtual ground. Given this fact, and the arrangement of the duty cycle modulator polarities internal to the PFC, an increase in positive current from the gain modulator will cause the output stage to increase its duty cycle until the voltage on ISENSE (pin8) is adequately negative to cancel this increased current. Similarly, if the gain modulator's output decreases, the output duty cycle will decrease, to achieve a less negative voltage on the ISENSE (pin8).

Error Amplifier Compensation

The PWM loading of the PFC can be modeled as a negative resistor; an increase in input voltage to the PWM causes a decrease in the input current. This response dictates the proper compensation of the two transconductance error amplifiers. Figure 1 shows the types of compensation networks most commonly used for the voltage and current error amplifiers, along with their respective return points. The current loop compensation is returned to V_{REF} (pin10) to produce a soft-start characteristic on the PFC: as the reference voltage comes up from zero volts, it creates a differentiated voltage on IEAO (pin9) which prevents the PFC from immediately demanding a full duty cycle on its boost converter.

Clean Digital PFC Brown Out

Clean Digital PFC Brown Out provides a clean cut off when AC input is much lower than regular AC input voltage such as 65Vac.

Inside of Clean Digital PFC Brown Out, there is a comparator monitors the internal Vrms voltage. Clean Digital PFC Brown Out inhibits the PFC and VEAO (pin4) (PFC error amplifier output) is pulled down when the internal Vrms is lower than off threshold, 1.0V (The off Vin voltage usually corresponds to 65Vac). When the internal Vrms voltage reaches 1.0625V (The On Vin voltage usually corresponds to 80Vac), PFC is on.

Cycle-By-Cycle Current Limiter and Selecting R_{SENSE}

The ISENSE (PIN8) (pin8), as well as being a part of the current feedback loop, is a direct input to the cycle-by-cycle current limiter for the PFC section. Should the input voltage at this pin ever be more negative than –1.25V, the output of the PFC will be disabled until the protection flip-flop is reset by the clock pulse at the start of the next PFC power cycle.

R_S is the sensing resistor of the PFC boost converter. During the steady state, line input current x R_{SENSE} = I_{mul} x 10K. Since the maximum output voltage of the gain modulator is I_{mul} max x 10K= 0.8V during the steady state, R_{SENSE} x line input current will be limited below 0.8V as well. When VEAO (pin4) reaches maximum VEAO (pin4) which is 5.5V, ISENSE (pin8) can reach -0.8V. At 100% load, VEAO (pin 4) should be around 3.75V and ISENSE (pin8) average peak is -0.51372V. It will provide the optimal dynamic response + tolerance of the components.

Therefore, to choose R_{SENSE}, we use the following equation:

R_{SENSE} + $R_{Parasitic}$ = 0.51372V x Vinpeak / (2 x Line Input power)

For example, if the minimum input voltage is 80VAC, and the maximum input rms power is 250Watt, R_{SENSE} + $R_{Parasitic}$ = (0.51372V x 80V x 1.414) / (2 x 250) = 0.116 ohm. The designer needs to consider the parasitic resistance and the margin of the power supply and dynamic response. Assume $R_{Parasitic}$ = 16 mOhm, R_{SENSE} = 100 mOhm.

3 voltage levels for PFC Boost Outputs (Patent Pending)

During Start Up to ensure the downstream SLS controller, CU6901V family having energy at Vcc, an extra 10uA current to GND will provide at Vfb (pin3). This extra 5uA will ensure CU6901V Vcc has the extra time to build up Vcc energy. For example, if normal PFC Boost Output ~ 380V, and Vfb (pin3) upper resistor value = 6 Mega ohm, during start up PFC Boost Output become ~ 380V + 6 Meg x 5uA = 410V. This extra 5uA at Vfb (pin3) is removed after ISOFT (pin5) > 2.5V.

When Veao (pin4) < 1.75V (with 500mV) hysteresis, 380V becomes ~ 355 when SD (pin6) < 3.0V. When Veao (pin4) > 2.5V, PFC Boost Output returns to 380V. This is the part of Dynamic Soft PFC actions. By doing so, the efficiency goes up.

PFC Voltage Loop

There are two major concerns when compensating the voltage loop error amplifier, VEAO (pin4); stability and transient response. Optimizing interaction between transient response and stability requires that the error amplifier's open-loop crossover frequency should be 1/2 that of the line frequency, or 23Hz for a 47Hz line (lowest anticipated international power frequency).

deviate from its 2.5V (nominal) value. If this happens, the transconductance of the voltage error amplifier, GMv will increase significantly, as shown in the Typical Performance Characteristics. This raises the gain-bandwidth product of the voltage loop, resulting in a much more rapid voltage loop response to such perturbations than would occur with a conventional linear gain characteristics.

The Voltage Loop Gain (S)

$$= \frac{\Delta V_{OUT}}{\Delta V_{EAO}} * \frac{\Delta V_{FB}}{\Delta V_{OUT}} * \frac{\Delta V_{EAO}}{\Delta V_{FB}}$$

$$\approx \frac{P_{IN} * 2.5V}{V_{OUTDC}^2 * \Delta V_{EAO} * S * C_{DC}} * GM_V * Z_{CV}$$

Z_{CV}: Compensation Net Work for the Voltage Loop
GMv: Transconductance of VEAO (pin4)
P_{IN}: Average PFC Input Power
V_{OUTDC}: PFC Boost Output Voltage; typical designed value is 380V.
C_{DC}: PFC Boost Output Capacitor

PFC Current Loop

The current transcondutance amplifier, GMi, IEAO (pin9) compensation is similar to that of the voltage error amplifier, VEAO (pin4) with exception of the choice of crossover frequency. The crossover frequency of the current amplifier should be at least 10 times that of the voltage amplifier, to prevent interaction with the voltage loop. It should also be limited to less than 1/6th that of the switching frequency, e.g. 8.33kHz for a 50kHz switching frequency.

PFC OVP

In the CU6500/02VA(B), PFC OVP comparator serves to protect the power circuit from being subjected to excessive voltages if the load should suddenly change. A resistor divider (typical total resistor value ~ 4Meg Ohm to ~ 10 Mega Ohm from the high voltage DC output of the PFC is fed to VFB (pin3). When the voltage on VFB (pin3) exceeds 2.75V, the PFC output driver is shut down. The PGB is still low to keep SLS, the downstream DC to DC converter continue to operate. The OVP comparator has 250mV of hysteresis, and the PFC will not restart until the voltage at VFB (pin3) drops below 2.54V.

The Current Loop Gain (S)

$$= \frac{\Delta V_{ISENSE}}{\Delta D_{OFF}} * \frac{\Delta D_{OFF}}{\Delta I_{EAO}} * \frac{\Delta I_{EAO}}{\Delta I_{SENSE}}$$

$$\approx \frac{V_{OUTDC} * R_S}{S * L * 2.5V} * GM_I * Z_{CI}$$

Z_{CI}: Compensation Net Work for the Current Loop
GM_I: Transconductance of IEAO (pin9)
V_{OUTDC}: PFC Boost Output Voltage; typical designed value is 380V and we use the worst condition to calculate the Z_{CI}
R_{SENSE}: The Sensing Resistor of the Boost Converter
2.5V: The Amplitude of the PFC Leading Edge Modulation Ramp(typical)
L: The Boost Inductor

The gain vs. input voltage of the CU6500/02VA(B)'s voltage error amplifier, VEAO (pin4) has a specially shaped non-linearity such that under steady-state operating conditions the transconductance of the error amplifier, GMv is at a local minimum. Rapid perturbation in line or load conditions will cause the input to the voltage error amplifier VFB (pin3) to

ISENSE (pin8) Filter, the RC filter between R_{SENSE} and ISENSE (pin8) :

There are 2 purposes to add a filter at ISENSE (pin8) pin:

1.) Protection: During start up or inrush current conditions, it will have a large voltage cross Rs which is the sensing resistor of the PFC boost converter. It requires the ISENSE (PIN8) Filter to attenuate the energy.
2.) To reduce L, the Boost Inductor: The ISENSE (pin8) Filter To reduce L, the Boost Inductor: The ISENSE (pin8) Filter also can reduce the Boost Inductor value since the ISENSE (pin8) Filter behaves like an integrator before going ISENSE (pin8) which is the input of the current error amplifier, IEAO (pin9).

The ISENSE (pin8) Filter is a RC filter. The resistor value of the ISENSE (pin8) Filter is 50 ohm because I_{OFFSET} x the resistor can generate an offset voltage of IEAO (PIN9). By selecting R_{FILTER} equal to 50ohm will keep the offset of the IEAO (pin9) less than 1mV. Usually, we design the pole of ISENSE (PIN8) Filter at fpfc/6~fpfc=8.33Khz, one sixth of the PFC switching frequency. Therefore, the boost inductor can be reduced 6 times without disturbing the stability. Therefore, the capacitor of the ISENSE (pin8) Filter, C_{FILTER}, will be around 382.1nF.

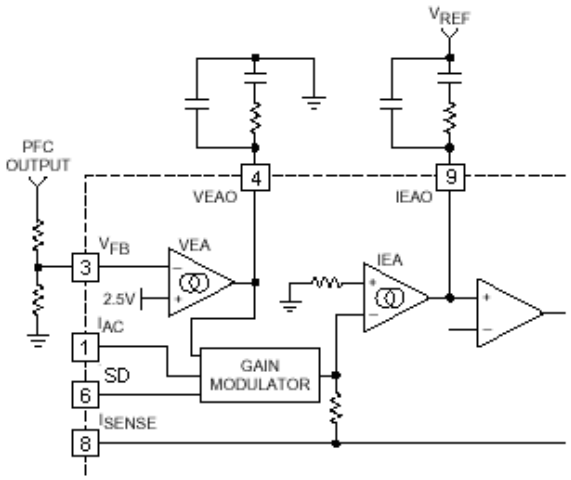


Figure 1. Compensation Network Connections for the Voltage and Current Error Amplifiers

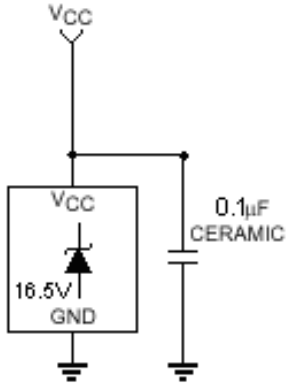


Figure 2. External Component Connections to V_{CC}

Internal Oscillator (RAMP1, or called RTCT)

In CU6500/02VA(B), frtct = fpfc = 67.5Khz, it is generated internally. The dead time of the oscillator determined PFC minimum off time which is ~ 457nS. RTCT ramp as the other PFC product from 1.25V to 3.75V.

Improve Efficiency at Super Light Load and No Load

When VEAO (pin13) < 0.75V and 1.0V (250mV hysteresis), switching frequency becomes ~ 25Khz to improve the super light load efficiency.

PFC Kick Mode (VEAO (pin4) < 0.45V)

When VEAO (pin4) <~ 0.45V, PFCOUT Stops. When VEAO (pin4) > ~ 0.45V, PFCOUT is enabled.

CU6901's SLS Kick Mode may interact with PFC Kick Mode to raise the level of the load going into Kick Mode. Increase the sensing resistor to Raise Veao (pin4) level or slow Veao by increasing the compensation capacitor value further to desensitize the interaction.

Increase Vfb (pin3) capacitor may or may not help here.

When SD > 6.0V with 1.7mS timer delay, "Latch" Mode is entered. Vcc will go up and down between 15.0V and 12.0V until AC input is removed and Vcc goes down below UVLOoff =10.0V, CU6500/02VA will retry again.

ISOFT (pin5)

There is a ~ 10uA to charge ISOFT (pin5). The PFC-soft-start function is implemented with ISOFT (pin5).

PGB (pin7) On/Off 6901V so it On/Off power supply

For CU6500/02VA:

PGB is designed to On/Off SLS controller, CU6901V. When Vfb > 2.25V, PGB is pulled low and when Vfb < 1.85V @ heavy load, PGB is pulled high. At light load, Vfb < 1.79V, PGB is pulled high. Usually, a 15K ohm resistor in series with an optical couple can source > 400uA.

Besides PGB is high when Vfb < 1.95V, when Vcc < UVLOoff = 10V, PGB is pulled high. Also, PGB is high when SD pin > 2.5V with 1.7mS delay.

For CU6500/02VB:

PGB is designed to On/Off SLS controller, CU6901V. When Vfb > 2.25V, PGB is pulled low and when Vfb < 1.95V @ heavy load, PGB is pulled high. At light load, Vfb < 1.89V, PGB is pulled high. Usually, a 15K ohm resistor in series with an optical couple can source > 400uA.

Besides PGB is high when Vfb < 1.95V, when Vcc < UVLOoff = 10V, PGB is pulled high. Also, PGB is high when SD pin > 2.5V with 1.7mS delay.

CU6500/02VA for AC Adapter Protection: "Retry" when SD (pin6) > 2.5V or "Latch" when SD (pin6) is pulled > 6.0V

When CU6500/02VA and CU6901V SLS system is designed for high end AC Adapter, CU6901V has a pin called FAULT (pin6). By using a low current optical couple, CU6901V FAULT (pin6) via optical couple to pull up SD (pin6) of CU6500/02VA. When **SD > 2.5V** with ~ 1.7mS delay, CU6500/02VA turns off PFCOUT gate driver, and pull up PGB (pin 7). When Vcc < UVLOoff = 10V, it retries again. It is called "Retry" Mode.

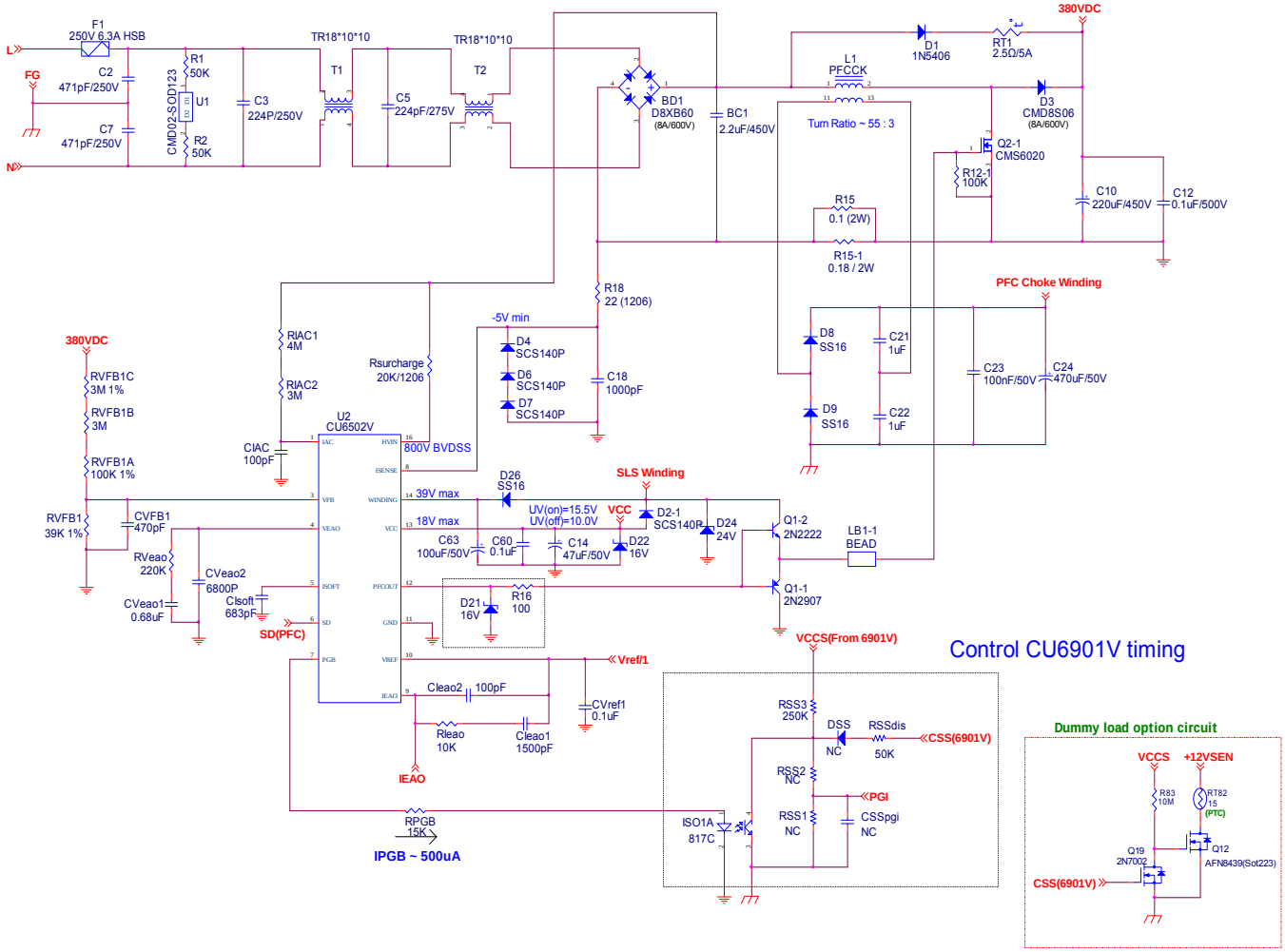
If **SD > 6.0V** with 1.7mS delay, CU6500/02VA turns off PFCOUT gate driver, pull up PGB (pin7) and Vcc goes up and down between ~ 15V and ~ 12V until AC input is removed and Vcc goes down below UVLOoff = 10.0V, power supply will retry again.

CU6500/02VB for AC Adapter Protection: "Latch" when SD (pin6) is pulled > 2.5V

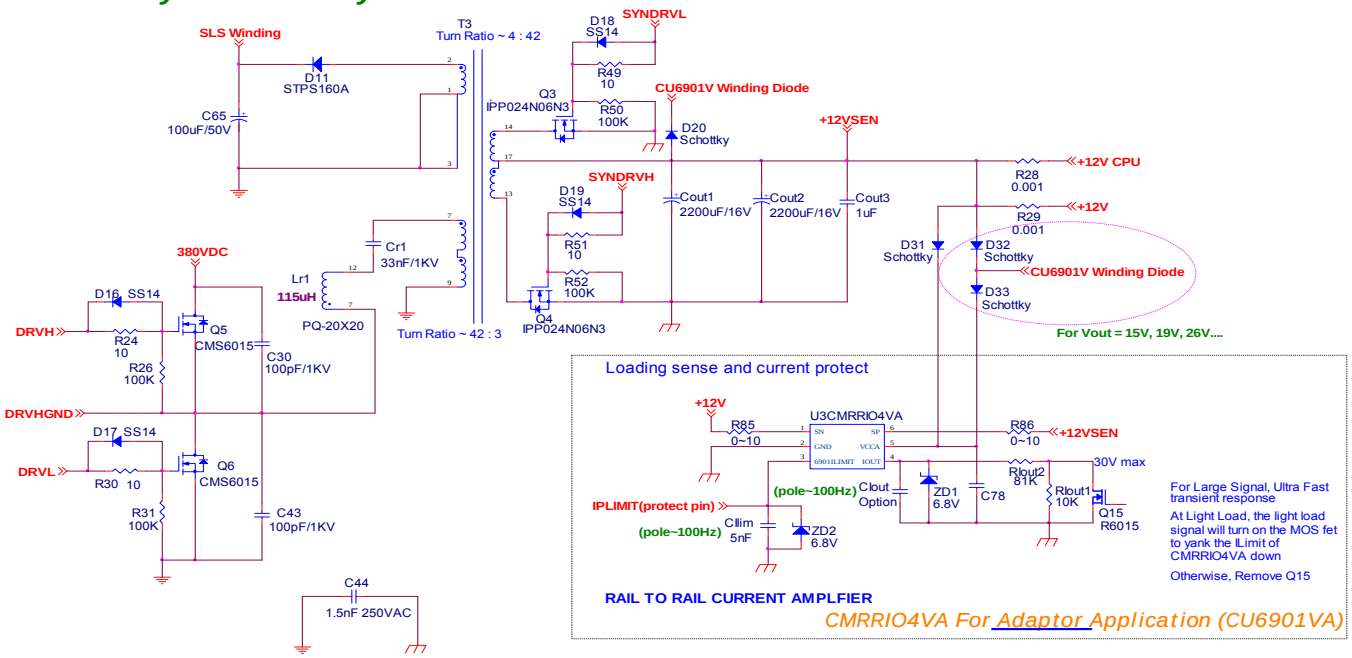
When CU6500/02VA and CU6901V SLS system is designed for high end AC Adapter, CU6901V has a pin called FAULT (pin6). By using a low current optical couple, CU6901V FAULT (pin6) via optical couple pulls up SD (pin6) of CU6500/02VA. When **SD > 2.5V** with 1.7mS delay, CU6500/02VB turns off PFCOUT gate driver, pull up PGB (pin7) and Vcc goes up and down between ~ 15V and ~ 12V until AC input is removed and Vcc goes down below UVLOoff = 10.0V, power supply will retry again.

TYPICAL APPLCATION CIRCUIT

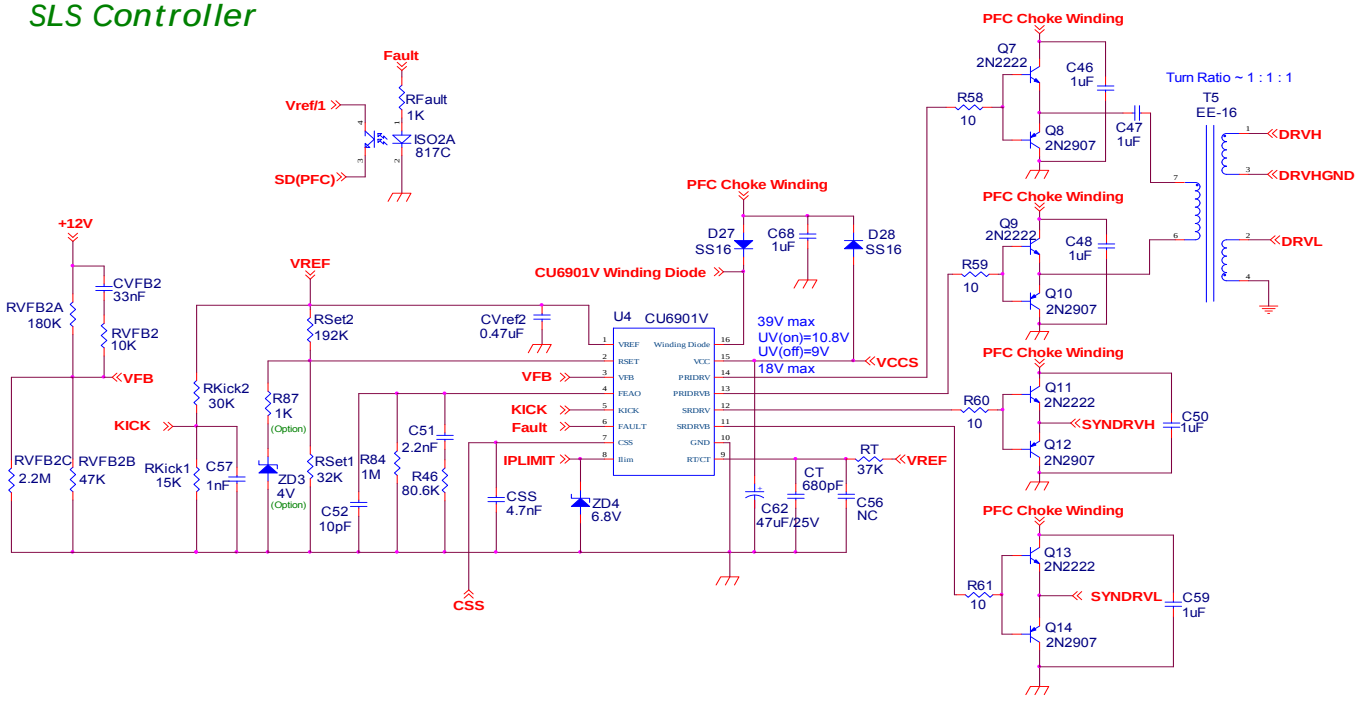
PFC Stage



Main Primary & Secondary

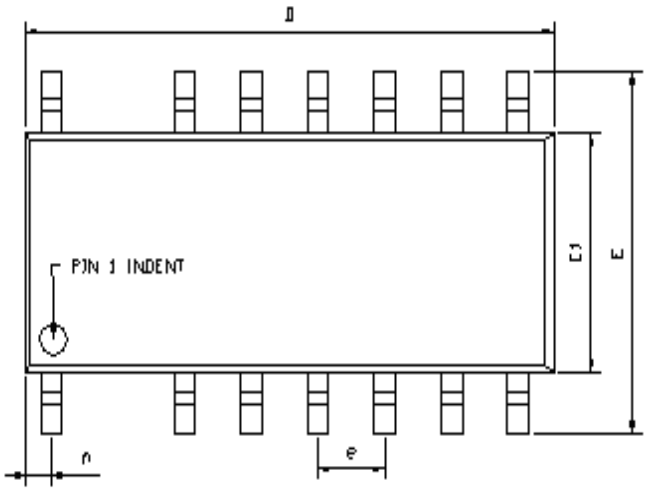


SLS Controller



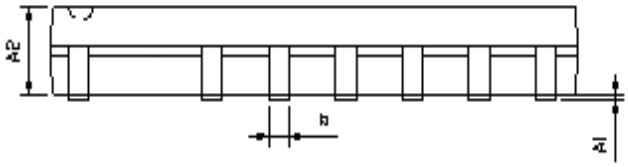
PACKAGE DIMENSION

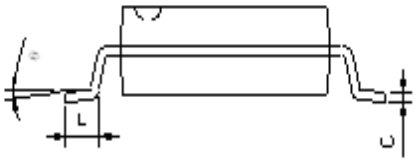
16-PIN SOP (S16)



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHS		
	MIN	NOM	MAX	MIN	NOM	MAX
A1	0.10	----	0.25	0.004	----	0.010
A2	1.40	----	1.55	0.055	----	0.061
b	0.30	----	0.51	0.012	----	0.020
C	0.15	----	0.26	0.006	----	0.010
D	9.80	----	10.06	0.386	----	0.396
E	5.79	----	6.20	0.228	----	0.244
E1	3.76	----	4.01	0.148	----	0.158
e	----	1.27	----	----	0.050	----
L	0.38	----	0.69	0.015	----	0.035
m	0.43	----	0.69	0.017	----	0.027
θ	0°	----	8°	0°	----	8°

EXPOSED PAD DIMENSION : (mm)
PAD SIZE: X=2.3 , Y=2.8





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