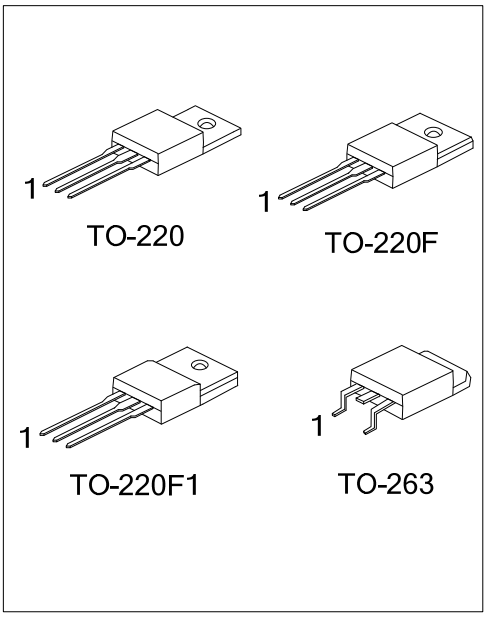
15A, 650V N-CHANNEL SUPER-JUNCTION MOSFET



■ DESCRIPTION

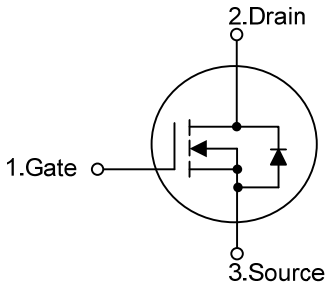
The UTC **15NM65-SH** is an Super Junction MOSFET Structure . It uses UTC advanced planar stripe, DMOS technology to provide customers perfect switching performance, minimal on-state resistance.

The UTC **15NM65-SH** is universally applied in electronic lamp ballasts based on half bridge topology, high efficiency switched mode power supplies, active power factor correction, etc.

■ FEATURES

* $R_{DS(ON)}$ < 0.35Ω @ V_{GS}=10V, I_D=7.5A
* By using Super Junction Structure
* Fast Switching
* With 100% Avalanche Tested

■ SYMBOL



■ ORDERING INFORMATION

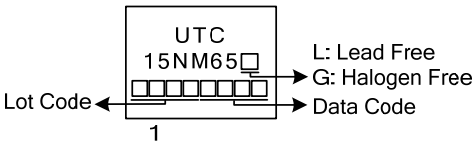
Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
15NM65L-TA3-T	15NM65G-TA3-T	TO-220	G	D	S	Tube
15NM65L-TF3-T	15NM65G-TF3-T	TO-220F	G	D	S	Tube
15NM65L-TF1-T	15NM65G-TF1-T	TO-220F1	G	D	S	Tube
15NM65L-TQ2-T	15NM65G-TQ2-T	TO-263	G	D	S	Tube
15NM65L-TQ2-R	15NM65G-TQ2-R	TO-263	G	D	S	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

15NM65L-TA3-T
(1) Packing Type
(2) Package Type
(3) Green Package

(1) T: Tube, R: Tape Reel
(2) TA3: TO-220, TF1: TO-220F1, TF3: TO-220F, TQ2: TO-263
(3) L: Lead Free, G: Halogen Free and Lead Free

■ MARKING



■ ABSOLUTE MAXIMUM RATINGS (T_C = 25°C, unless otherwise specified)

PARAMETER			SYMBOL	RATINGS	UNIT
Drain to Source Voltage			V_{DSS}	650	V
Gate to Source Voltage			V_{GSS}	±30	V
Continuous Drain Current		T_C=25°C	I_D	15 (Note 2)	A
		T_C=100°C		7 (Note 2)	A
Pulsed Drain Current (Note 3)			I_{DM}	44 (Note 2)	A
Single Pulsed Avalanche Energy(Note 4)			E_{AS}	715	mJ
Peak Diode Recovery dv/dt (Note 5)			dv/dt	4.5	V/ns
Power Dissipation	(T_C=25°C)	TO-220F/TO-220F1	P_D	38.5	W
		TO-220/TO-263		250	W
	Derate above 25°C	TO-220F/TO-220F1		0.3	W/°C
		TO-220/TO-263		2.0	W/°C
Junction Temperature			T_J	+150	°C
Storage Temperature			T_{STG}	-55 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. Drain current limited by maximum junction temperature
3. Repetitive Rating : Pulse width limited by maximum junction temperature
4. L=159mH, I_{AS}=3A, V_{DD}= 50V, R_G=25Ω, Starting T_J=25°C
5. I_{SD} ≤11A, di/dt ≤200A/μs, V_{DD} ≤BV_{DSS}, Starting T_J=25°C

■ THERMAL DATA

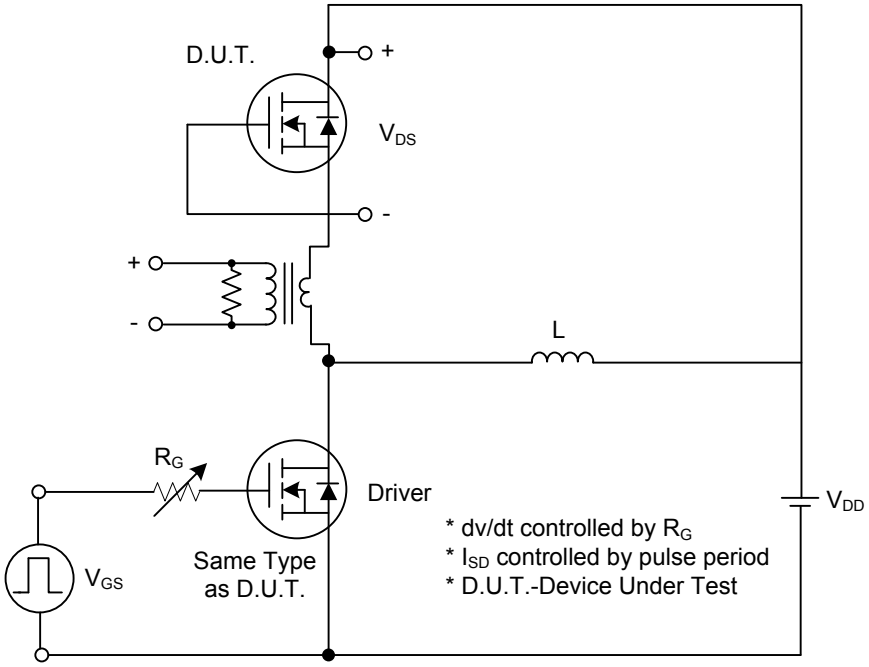
PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient		θ_{JA}	62.5	°C/W
Junction to Case	TO-220F/TO-220F1	θ_{JC}	3.3	°C/W
	TO-220/TO-263		0.5	°C/W

■ ELECTRICAL CHARACTERISTICS (T_C=25°C, unless otherwise specified)

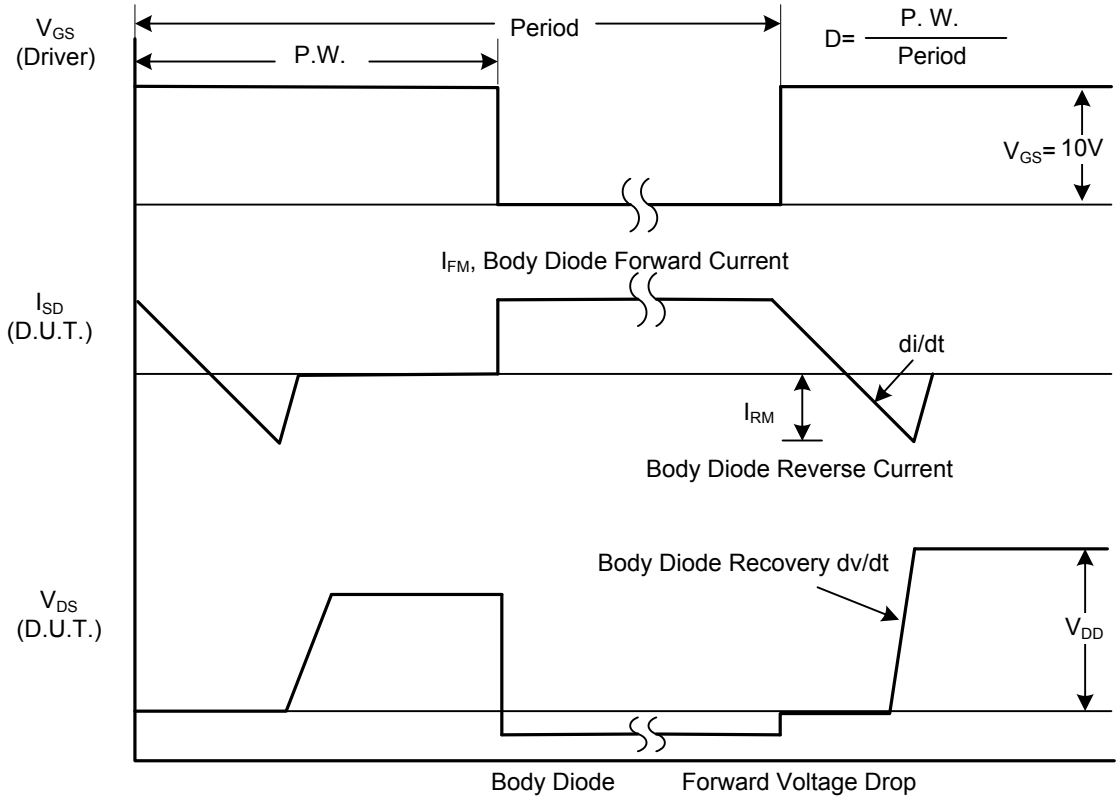
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=250μA	650			V
Breakdown Voltage Temperature Coefficient	$\Delta BV_{DSS}/\Delta T_J$	I_D=250μA,Referenced to 25°C		0.5		V/°C
Drain-Source Leakage Current	I_{DSS}	V_{DS}=650V, V_{GS}=0V			10	μA
		V_{DS}=650V, T_J=125°C			100	μA
Gate-Source Leakage Current	I_{GSS}	V_{DS}=0V ,V_{GS}=±30V			±100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS}= V_{GS}, I_D=250μA	2.5		4.5	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=7.5A		0.27	0.35	Ω
DYNAMIC PARAMETERS						
Input Capacitance	C_{ISS}	V_{DS}=25V,V_{GS}=0V, f=1.0MHz		1140		pF
Output Capacitance	C_{OSS}			500		pF
Reverse Transfer Capacitance	C_{RSS}			18		pF
SWITCHING PARAMETERS						
Turn-ON Delay Time	$t_{D(ON)}$	V_{DD}=30V, I_D=0.5A, R_G=25Ω V_{GS}=10V (Note 1, 2)		78		ns
Turn-ON Rise Time	t_R			140		ns
Turn-OFF Delay Time	$t_{D(OFF)}$			262		ns
Turn-OFF Fall Time	t_F			132		ns
Total Gate Charge	Q_G	V_{DS}=50V, V_{GS}=10V, I_D=1.3A , I_G=100μA (Note 1, 2)		140		nC
Gate-Source Charge	Q_{GS}			10		nC
Gate-Drain Charge	Q_{GD}			25		nC
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Maximum Body-Diode Continuous Current	I_S				11	A
Maximum Body-Diode Pulsed Current	I_{SM}				44	A
Drain-Source Diode Forward Voltage	V_{SD}	I_S =15A, V_{GS}=0V			1.4	V

Notes: 1. Pulse Test : Pulse width ≤ 300μs, Duty cycle ≤ 2%
2. Essentially independent of operating temperature

■ TEST CIRCUITS AND WAVEFORMS

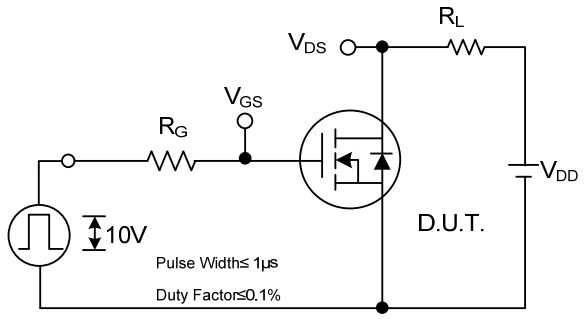


Peak Diode Recovery dv/dt Test Circuit

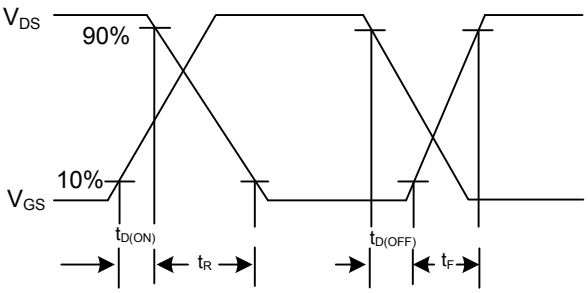


Peak Diode Recovery dv/dt Waveforms

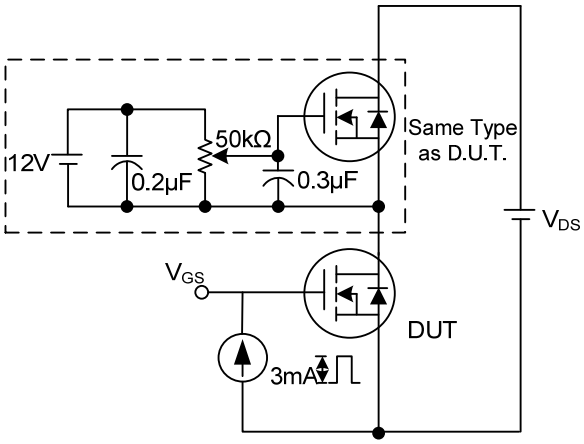
■ TEST CIRCUITS AND WAVEFORMS (Cont.)



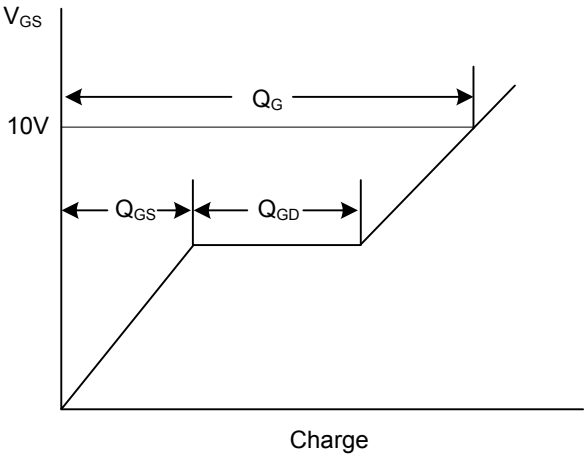
Switching Test Circuit



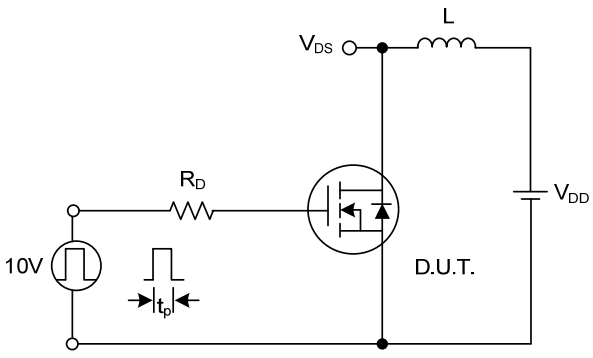
Switching Waveforms



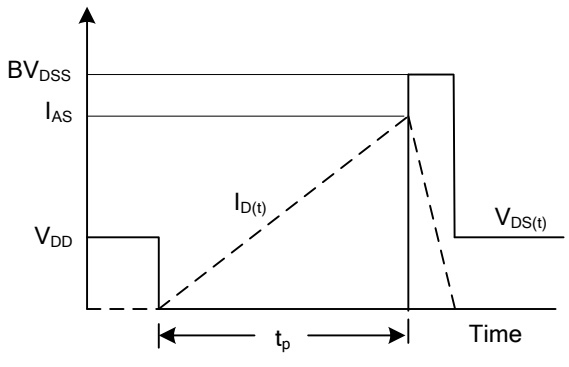
Gate Charge Test Circuit



Gate Charge Waveform



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms