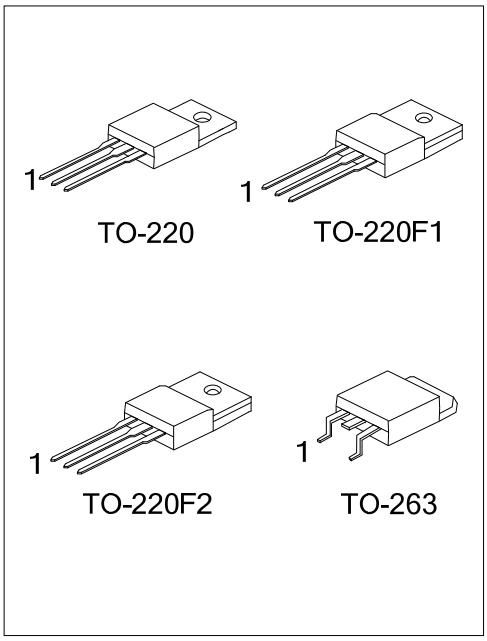
12A, 650V N-CHANNEL POWER MOSFET



■ DESCRIPTION

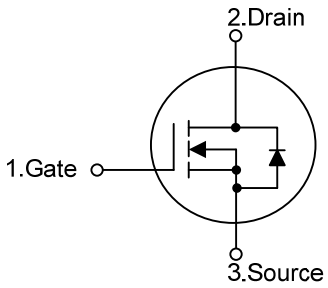
The UTC **12N65K-MT** are N-Channel enhancement mode power field effect transistors (MOSFET) which are produced by using UTC's proprietary, planar stripe and DMOS technology.

These devices are suited for high efficiency switch mode power supply. To minimize on-state resistance, provide superior switching performance and withstand high energy pulse in the avalanche and commutation mode, the advanced technology has been especially tailored.

■ FEATURES

* $R_{DS(ON)}$ < 0.75 Ω @ V_{GS} = 10 V, I_D = 6 A
* Fast switching capability
* Avalanche energy specified
* Improved dv/dt capability, high ruggedness

■ SYMBOL



■ ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
12N65KL-TA3-T	12N65KG-TA3-T	TO-220	G	D	S	Tube
12N65KL-TF1-T	12N65KG-TF1-T	TO-220F1	G	D	S	Tube
12N65KL-TF2-T	12N65KG-TF2-T	TO-220F2	G	D	S	Tube
12N65KL-TQ2-T	12N65KG-TQ2-T	TO-263	G	D	S	Tube
12N65KL-TQ2-R	12N65KG-TQ2-R	TO-263	G	D	S	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

12N65KL-TF1-T (1)Packing Type (2)Package Type (3)Green Package	(1) T: Tube (2) TA3: TO-220, TF1: TO-220F1, TF2: TO-220F2 TQ2: TO-263 (3) L: Lead Free, G: Halogen Free and Lead Free

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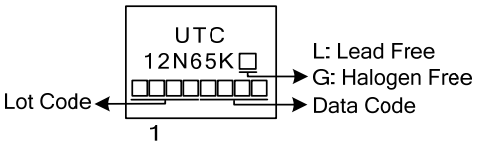
■ MARKING



■ ABSOLUTE MAXIMUM RATINGS (T_C = 25°C, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	650	V
Gate-Source Voltage		V_{GSS}	±30	V
Drain Current	Continuous	I_D	12	A
	Pulsed (Note 2)	I_{DM}	48	A
Avalanche Energy	Single Pulsed (Note 3)	E_{AS}	400	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	2.7	V/ns
Power Dissipation	TO-220/TO-263	P_D	51	W
	TO-220F1/TO-220F2		225	W
Junction Temperature		T_J	+150	°C
Operating Temperature		T_{OPR}	-55 ~ +150	°C
Storage Temperature		T_{STG}	-55 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. Repetitive Rating : Pulse width limited by maximum junction temperature
3. L = 5.55mH, I_{AS} = 12A, V_{DD} = 50V, R_G = 25Ω, Starting T_J = 25°C
4. I_{SD} ≤ 12A, di/dt ≤200A/μs, V_{DD} ≤BV_{DSS} Starting T_J = 25°C

■ THERMAL DATA

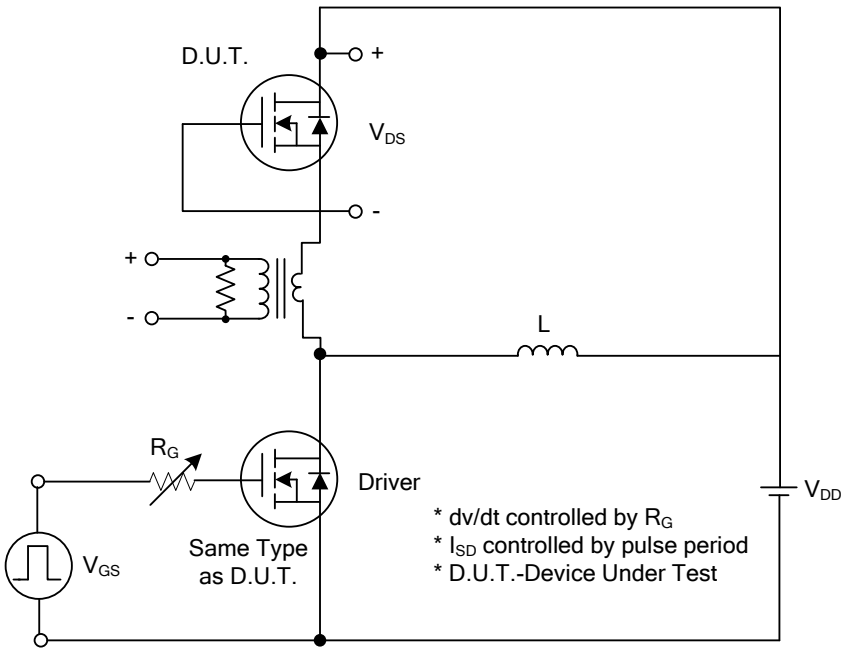
PARAMETER		SYMBOL	RATING	UNIT
Junction to Ambient		θ_{JA}	62.5	°C/W
Junction to Case	TO-220/TO-263	θ_{JC}	0.56	°C/W
	TO-220F1/TO-220F2		2.43	°C/W

■ ELECTRICAL CHARACTERISTICS (T_C =25°C, unless otherwise specified)

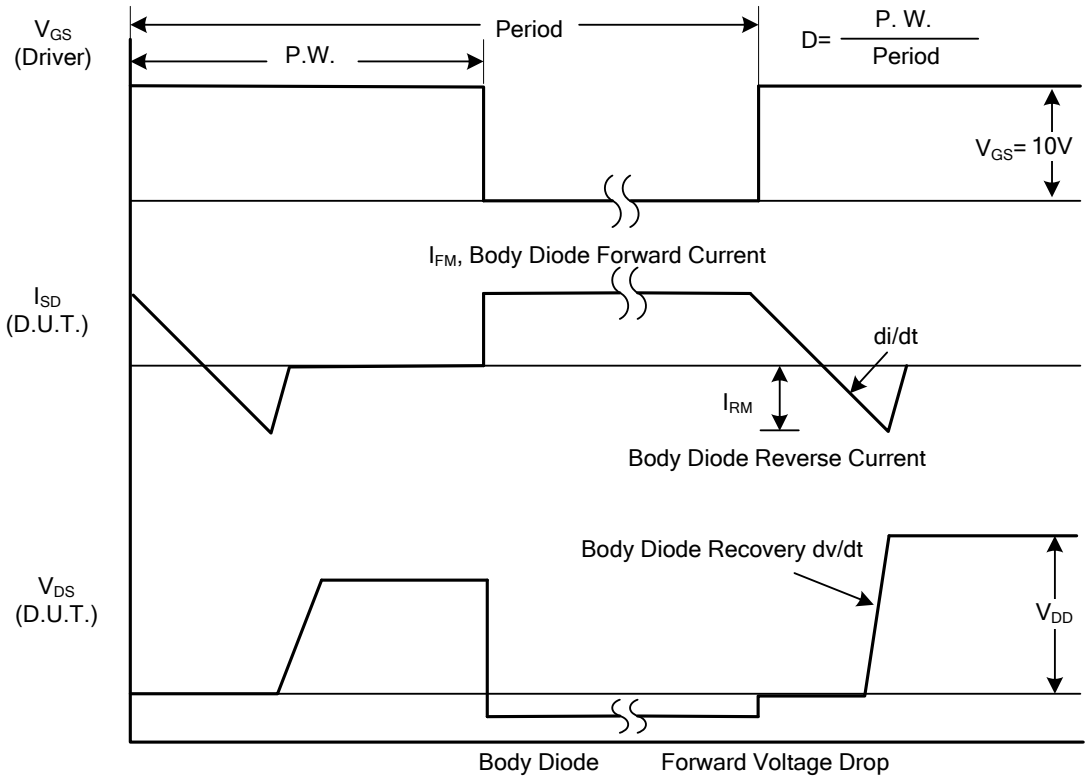
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0 V, I_D = 250 μA	650			V
Drain-Source Leakage Current	I_{DSS}	V_{DS} = 650 V, V_{GS} = 0 V			1	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±30 V, V_{DS} = 0 V			±100	nA
Breakdown Voltage Temperature Coefficient	$\triangle BV_{DSS}/\triangle T_J$	I_D=250μA,Referenced to 25°C		0.7		V/°C
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250μA	2.0		4.0	V
Static Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS} = 10V, I_D = 6.0A		0.60	0.75	Ω
DYNAMIC CHARACTERISTICS						
Input Capacitance	C_{ISS}	V_{DS} = 25 V, V_{GS} = 0 V, f = 1MHz		1600	1900	pF
Output Capacitance	C_{OSS}			175	210	pF
Reverse Transfer Capacitance	C_{RSS}			10	22	pF
SWITCHING CHARACTERISTICS						
Turn-On Delay Time	$t_{D(ON)}$	V_{DD} = 30V, I_D = 0.5A, R_G = 25Ω (Note 1, 2)		100	110	ns
Turn-On Rise Time	t_R			125	138	ns
Turn-Off Delay Time	$t_{D(OFF)}$			180	230	ns
Turn-Off Fall Time	t_F			104	140	ns
Total Gate Charge	Q_G	V_{DS}= 50V,I_D= 1.3A, V_{GS}= 10 V (Note 1, 2)		39	54	nC
Gate-Source Charge	Q_{GS}			10		nC
Gate-Drain Charge	Q_{GD}			9		nC
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Maximum Continuous Drain-Source Diode Forward Current	I_S				12	A
Maximum Pulsed Drain-Source Diode Forward Current	I_{SM}				48	A
Drain-Source Diode Forward Voltage	V_{SD}	V_{GS} = 0 V, I_S = 12A			1.4	V
Reverse Recovery Time	t_{rr}	I_S=12A, V_{GS}=0V di/dt=100A/μs (Note 1)		590		ns
Reverse Recovery Charge	Q_{RR}			6.2		μC

Notes: 1. Pulse Test : Pulse width ≤300μs, Duty cycle ≤ 2%
2. Essentially independent of operating temperature

■ TEST CIRCUITS AND WAVEFORMS

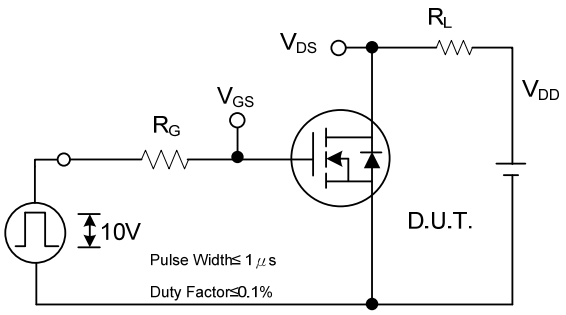


Peak Diode Recovery dv/dt Test Circuit

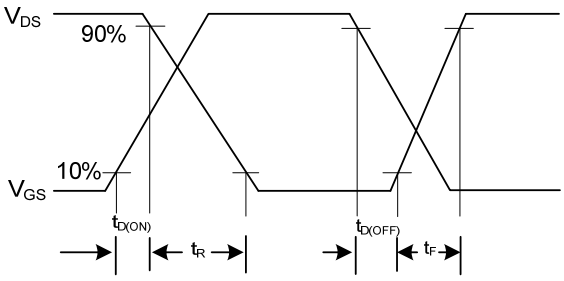


Peak Diode Recovery dv/dt Waveforms

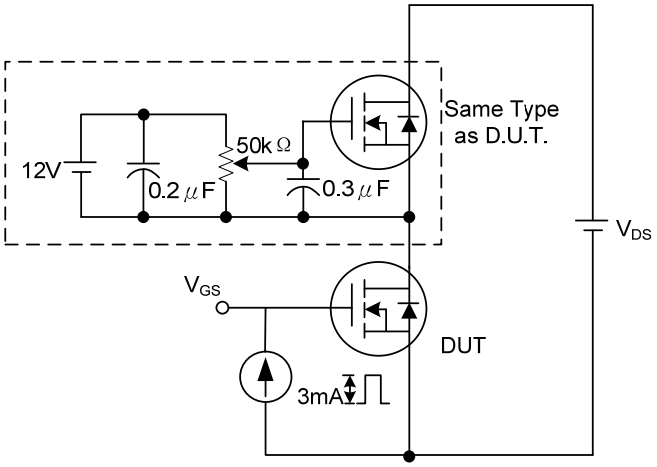
■ TEST CIRCUITS AND WAVEFORMS (Cont.)



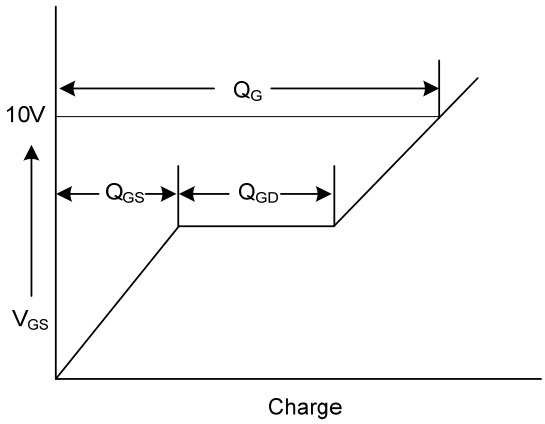
Switching Test Circuit



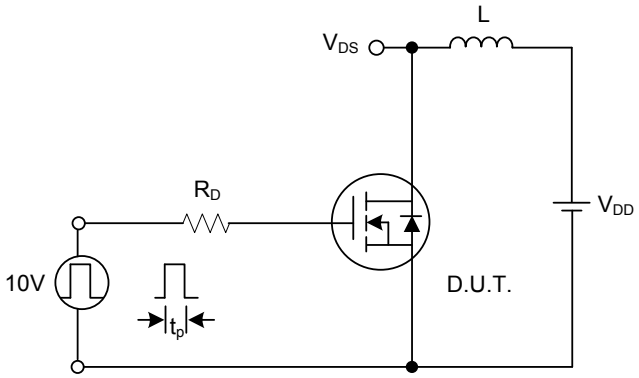
Switching Waveforms



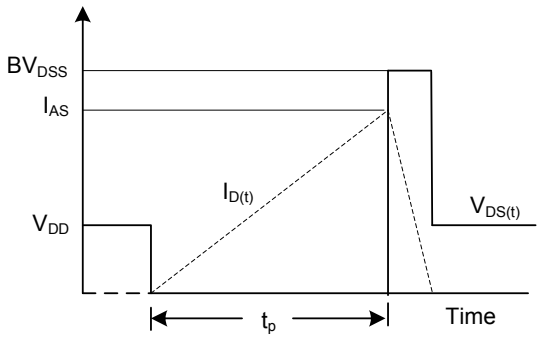
Gate Charge Test Circuit



Gate Charge Waveform



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

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